

Tentative**IMX294 Support Package**

The data except this specification conform to that of IMX294.

1. Description

This support package is intended to support product development for IMX294.

2. Description Items

- ◆ Guideline for designing the printed circuit board
- ◆ SLVS-EC
 - ◆ SLVS-EC overview
- ◆ MIPI
 - ◆ CSI-2 output
- ◆ Communication port
 - ◆ 3-wire serial
 - ◆ I²C
- ◆ Notes on clamp use
 - ◆ Sensor Internal Clamp and User Clamp
- ◆ Pattern Generator (PG) function
- ◆ Lens design guideline
- ◆ FAQ

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

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3. Guideline for designing the printed circuit board

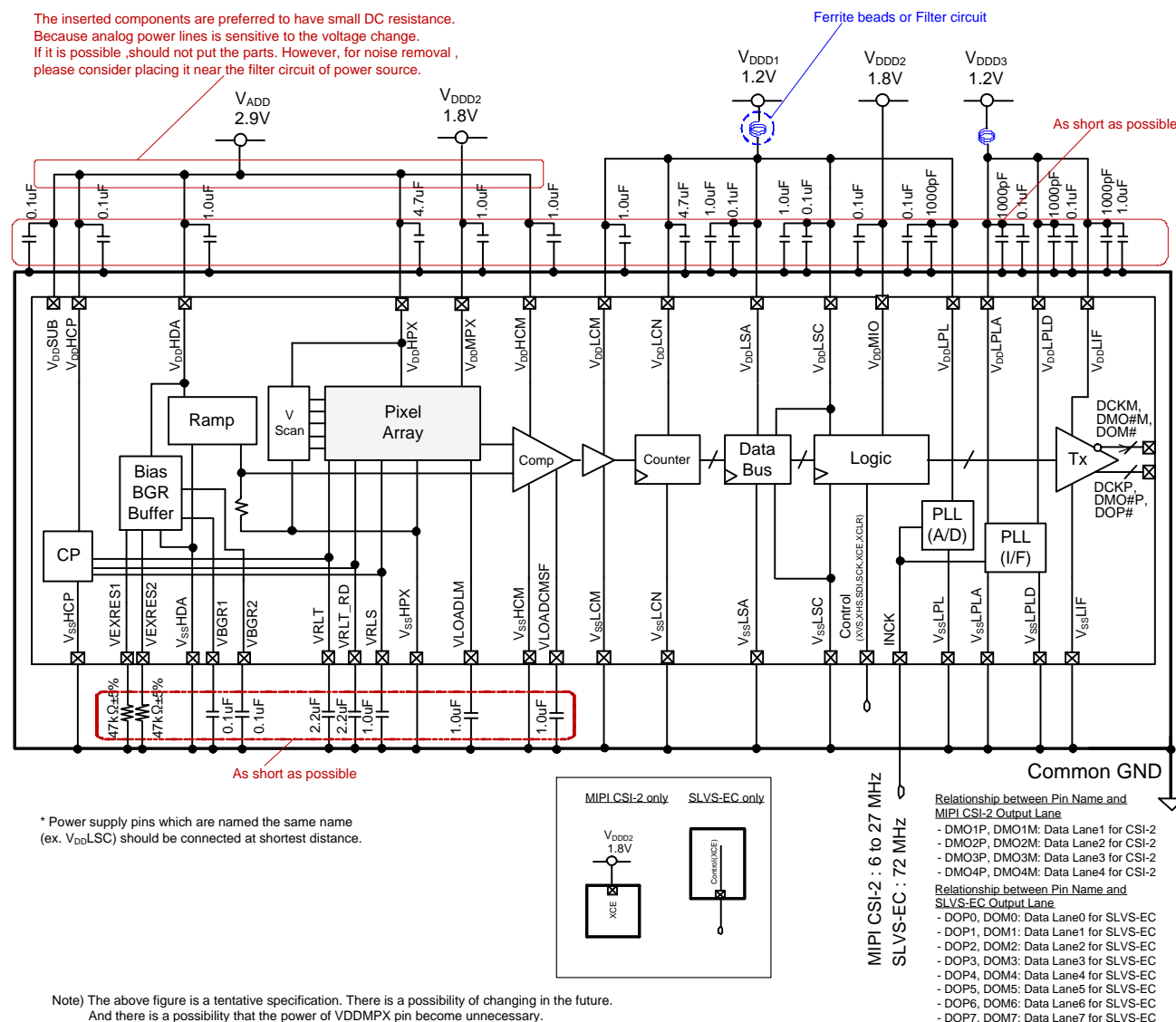
In this section we explain the design guideline of the printed circuit board layout and mount.

3.1. IMX294 Application circuit

3.1.1 Power supply pins

1. Please design the suitable filter in power supply line to reduce influence of a power supply noise and to prevent an unnecessary radiation. Especially, the parts to analog power supply pin need to choose the one that is small direct current resistance because that pin is sensitive to the voltage change. The voltage change becomes the factor of horizontal line noise.
2. We suggest that the use of reasonable noise filters on the power-line for suppressing the radiation noise from the lines.
3. Please mount peripheral parts (capacitor) near the element as much as possible.
4. Please make patterns of Power supply (2.9V, 1.8V, 1.2V) as wide as possible.
5. Please choose the capacity values according to application circuit.

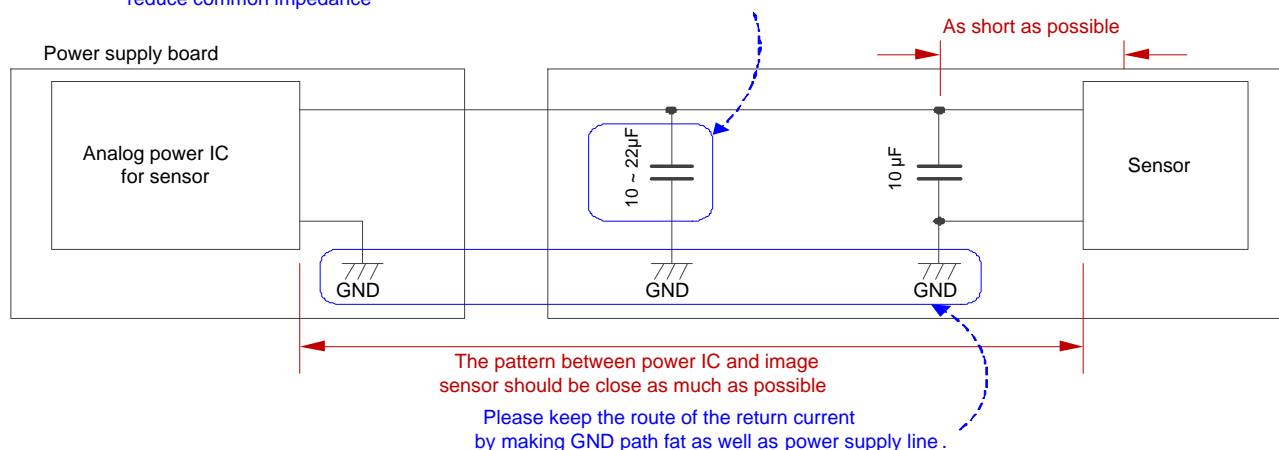
The inserted components are preferred to have small DC resistance.
Because analog power lines is sensitive to the voltage change.
If it is possible ,should not put the parts. However, for noise removal ,
please consider placing it near the filter circuit of power source.



Reference Design for Power Supply Pins

- We recommend to implement the power supply IC as close to the sensor as possible. If cannot, use wider power supply pattern of lower DC resistance, implement the large (10uF or more) decoupling capacitor close to the sensor. With regard to pattern, please refer to "Notes for designing pattern of printed circuit board".

Wiring length :10 cm (If it is possible), Bypass capacitor : 10 ~ 22μF (If necessary)
It is preferable to put capacitor separately in each power pin If you bring power line together , please bring it together near the IC , and make pattern wide to reduce common impedance



Layout of Power Supply IC and Decoupling Capacitors of Large Capacity

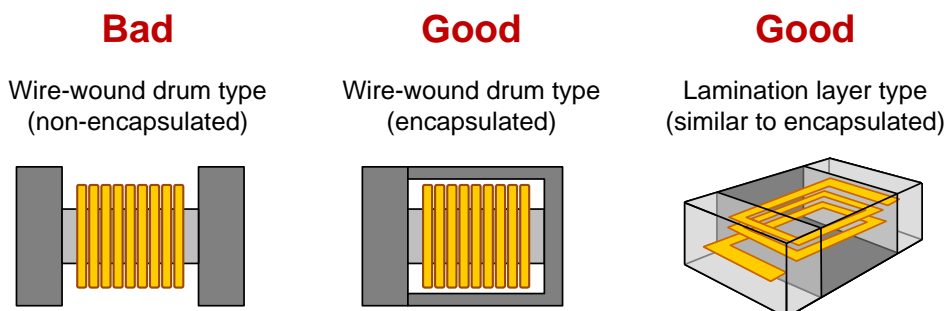
3.2. (Reference) Component

The following describes the components used reference information. When in actual use, please contact the manufacture for each component.

3.2.1. Power supply IC

Please select the power supply IC of better PSRR characteristics. Fluctuation of the power supply voltage will cause the horizontal line noise. In that case, we recommend that you use a series regulator. Please note that when using switching power regulator of the following points.

- When using switching power regulator, magnetic field induced by inductor might cause the noise of the image.
- Encapsulated (shield) type inductor is recommended.
- Mounting direction of the inductor also affects (increase or decrease) the noise level.



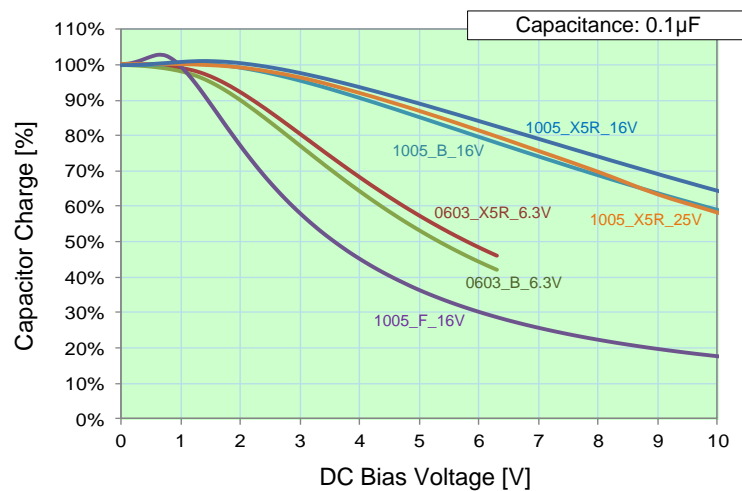
Encapsulated / Non-encapsulated Type Inductor

3.2.2. Decoupling capacitors

Please use non-polar capacitors. It is possible to operate the sensor by using typical ceramic capacitors.

1. All the power supply voltage are smaller than $2.9 \pm 0.1V$ so you can use any 1608M size capacitors of any characteristics in the graph. When you use 1005M size capacitors, you should select characteristics-B device. Characteristics-F device should not be chosen.
2. Decoupling capacitors for each pin are sensitive to image quality. Please implement sufficient capacity of the decoupling capacitors according to the power supply condition. If you use capacity that is small one and large one, please put the small one near the sensor. Please refer to Application circuit for details.
3. The capacity of the multilayer ceramic capacitors will decrease in regard to the impressed DC bias voltage. It will be more obvious when using smaller size and larger capacity, please check the specification sheet of each devices.

(Graph below shows the characteristics.)

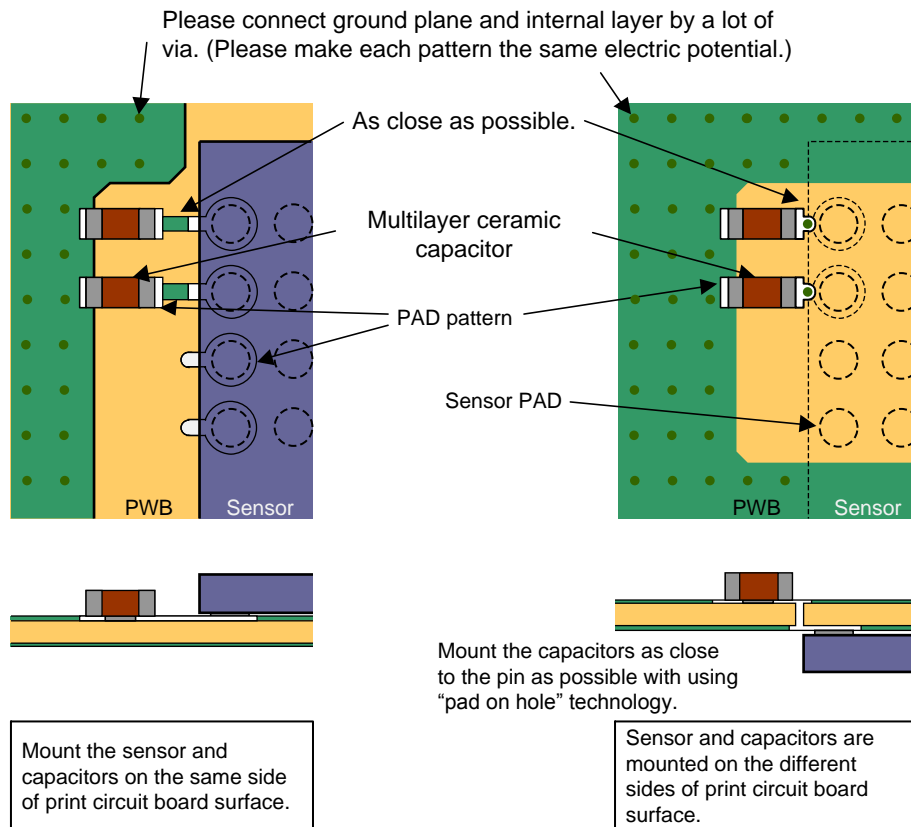


DC bias vs. Capacity

3.3. Notes for designing patterns of printed circuit board

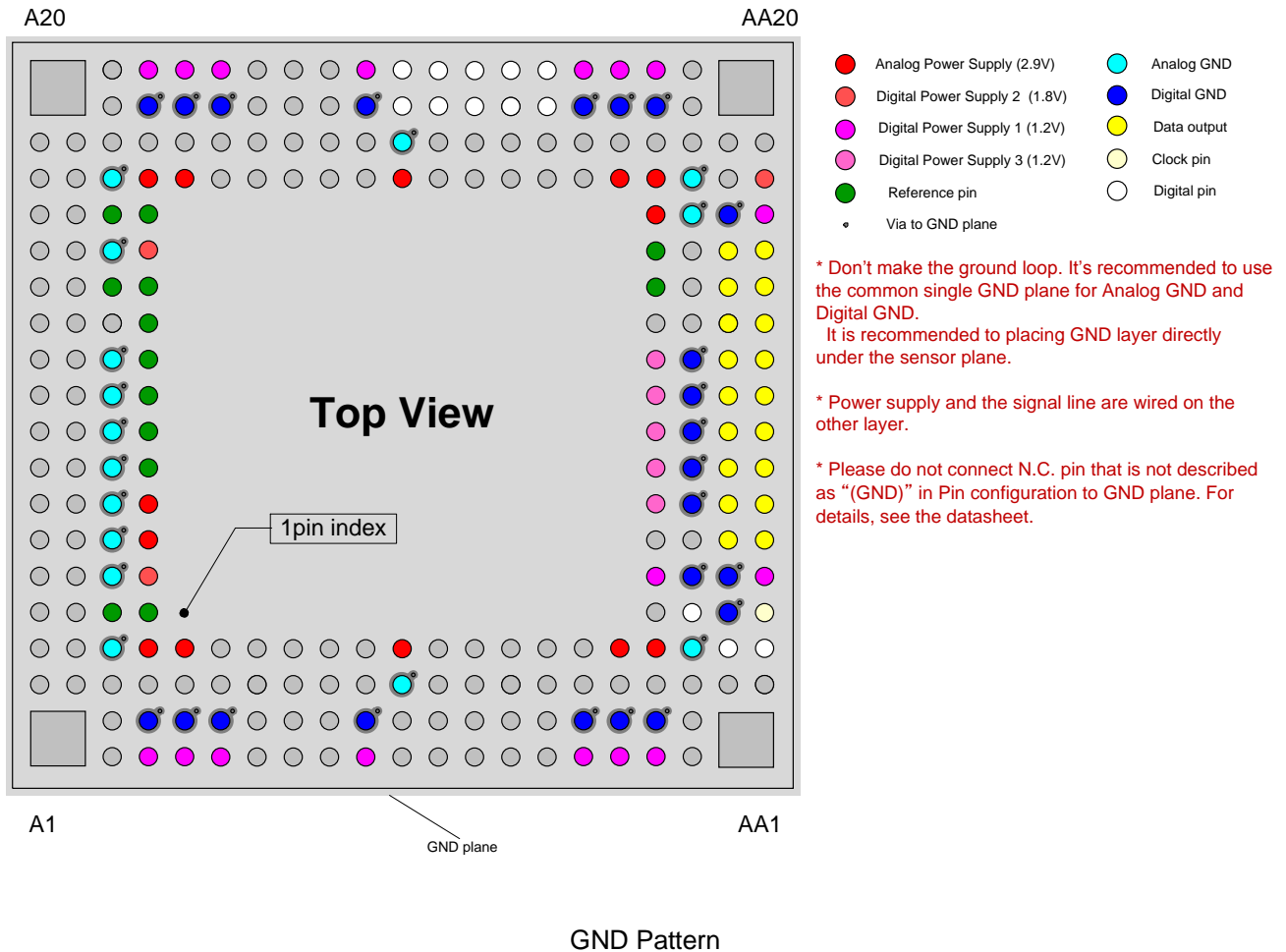
3.3.1. Power supply pins

1. The peripheral devices (capacitors) of the sensor should be mounted as close to the power supply pins as possible. Longer wire length might cause the degradation of the image quality.
2. Surface power/ground plane and inner layer power/ground plane should be connected with enough number of the vias (Vertical Interconnect Access) . Please make each pattern the same electric potential.



Example of Capacitor Mounting

3. Analog power supply pin is to receive the output image easy to be affected to the terminal noise. Please do not decrease from the capacity according to the application circuit example.
4. Loop of the ground pattern might propagate the noise to the other patterns (ex. Power supply pattern) so the ground pattern recommends Land pattern. It is recommended to use the common single GND plane for Analog GND and Digital GND.



5. Digital signal pattern on the other layer should not be in parallel with the power supply patterns, terminals of VRLS, VRLT and athores these lines.

3.4. Board design guidelines for SLVS-EC Interface

About these Guidelines

- These guidelines describe recommendations and notes regarding board layout design in order to obtain good electrical characteristics in an SLVS-EC interface.
- Values noted in these guidelines may need to be reconsidered depending on various conditions such as the materials, layer configuration and components actually used. Therefore, when designing the SLVS-EC board layout, it is strongly recommended to check the signal and power integrity using a parasitic parameter extraction tool, circuit simulations and other tools, and to select and check the ideal values at the customer's responsibility.
- In addition, these guidelines do not guarantee operation under all operating conditions.

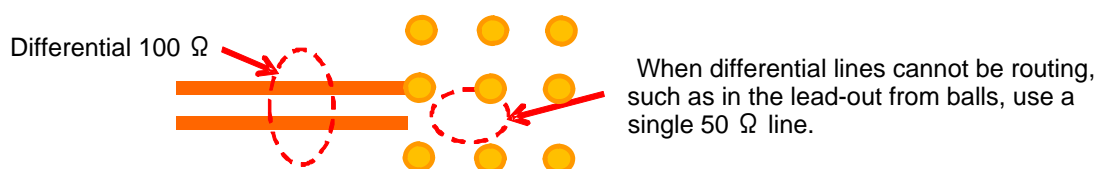
3.4.1. Guidelines for Transmission Line

1. transmission line

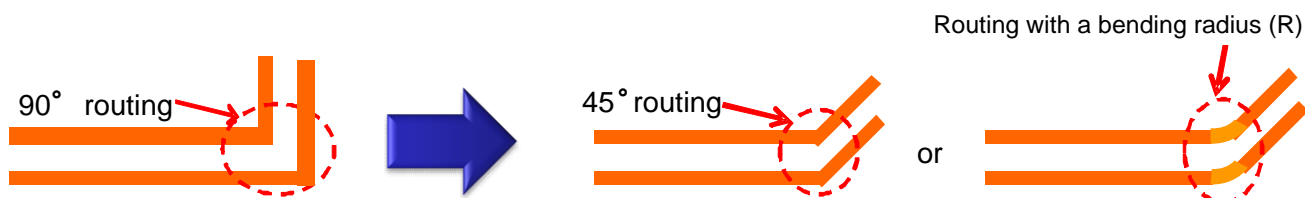
Use the line and space values guaranteed by the board manufacturer for a differential of 100 Ω . The allowable impedance tolerance is $100 \pm 10 \Omega$.

In locations where differential lines cannot be routed, route using the line and space values for single 50 Ω (BGA ball edges, etc.)

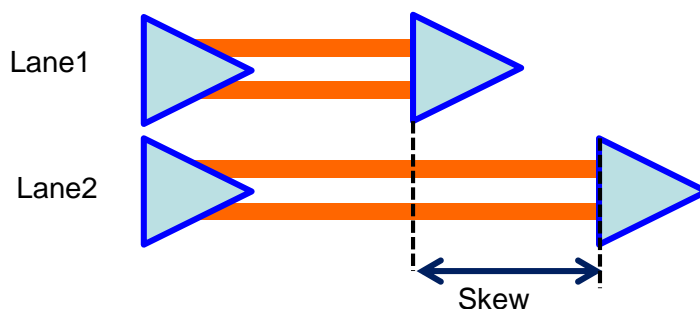
Use the routing layout that results in the shortest routing possible.



When bending a transfer path, do not bend the routing at 90°. Instead, use 45° routing or establish a bending radius (R).



Differential pair (positive/negative) lines should use equal-length routing (routing length difference: 1 mm or less). There is no need to make each lane equal length, but see the SLVS-EC Standard for the allowable skew.



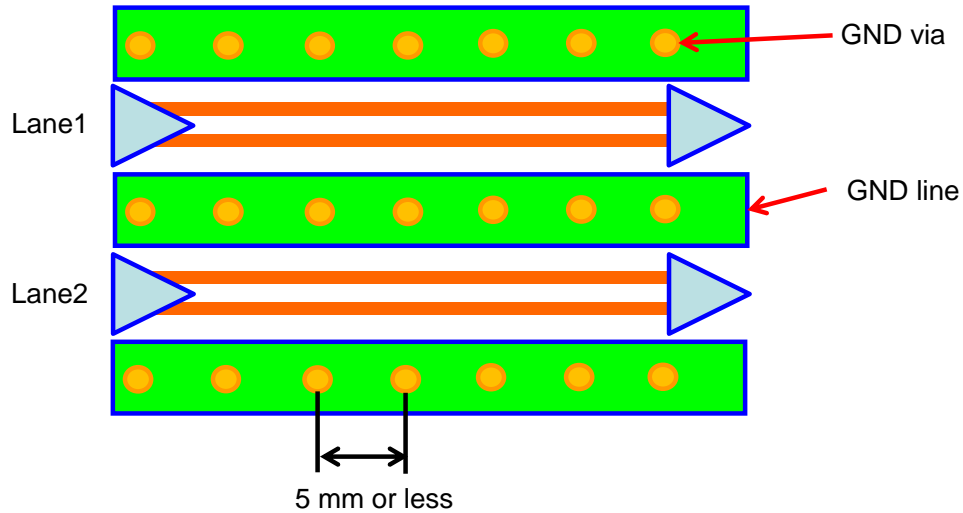
2. GND Line

Insert a GND line between differential lanes to reduce crosstalk.

When it is physically impossible to insert a GND line, separate the lanes. (Guideline: 3 times the lane width)

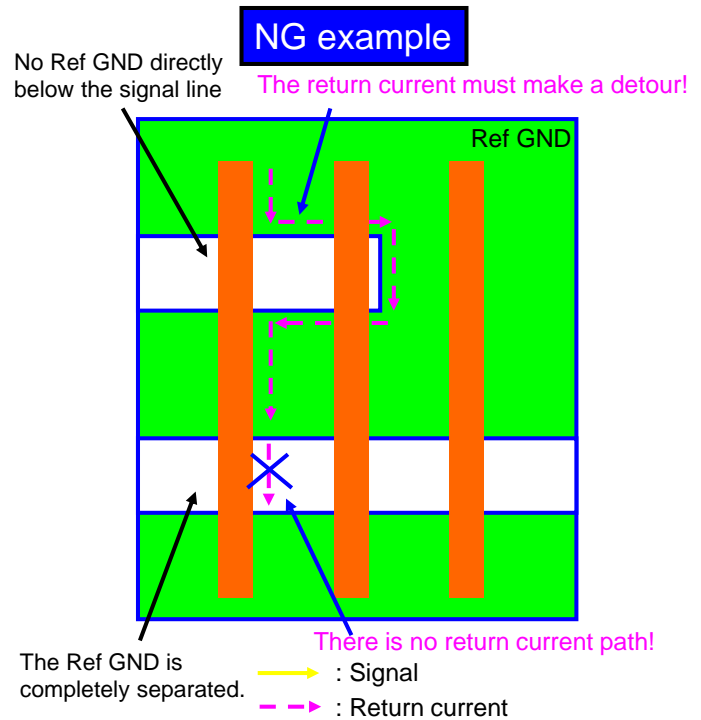
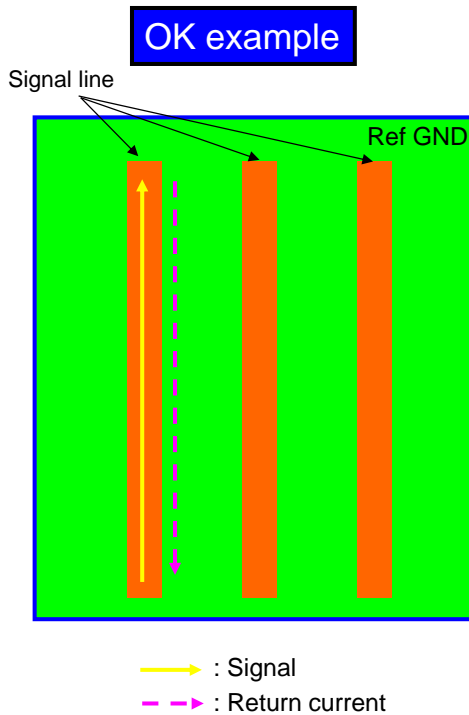
3. Through-hole Placement

Locate through-hole via (GND via) that connect to the solid GND on the L2 layer at intervals of 5 mm or less in the GND lines inserted in 2 above.



3.4.2. Notes on the Reference (Ref) GND

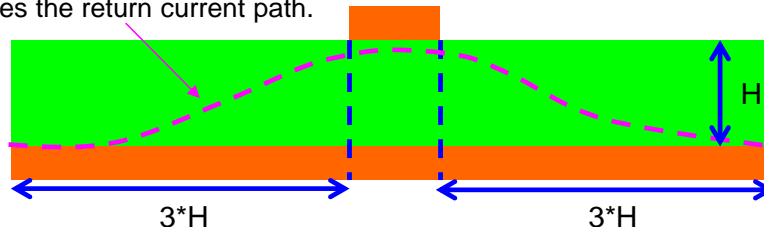
1. GND Plane to be Secured for the Return Current Path



2. Ref GND Plane

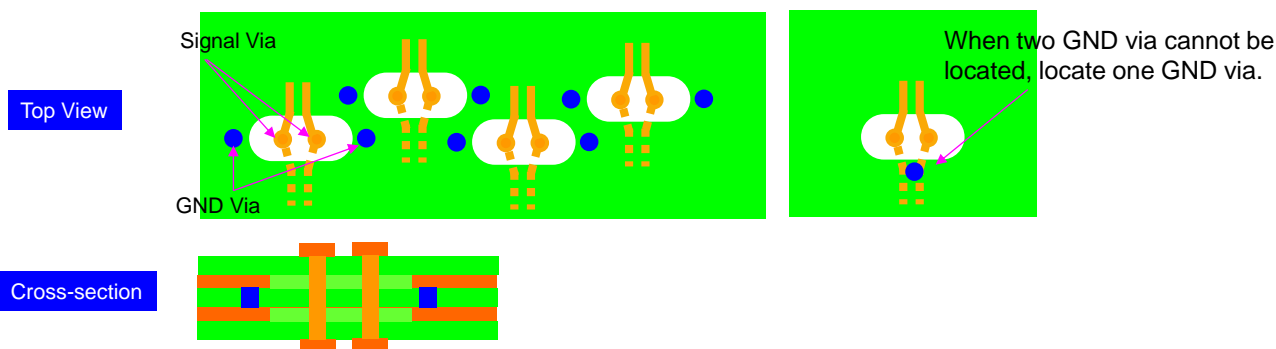
Secure a GND plane on both sides for 3 times or more the thickness (H) of the insulator (guideline).

This becomes the return current path.



3. GND Via

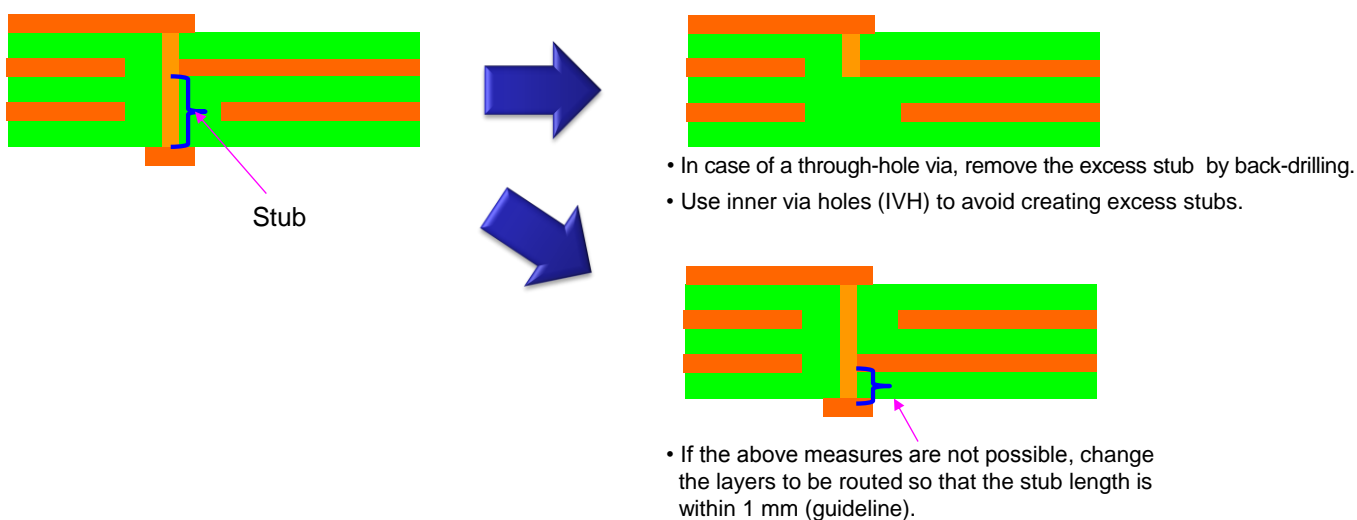
When it is necessary to route a signal line to a different layer through a via, locate GND via for the return current.



3.4.3. Notes on the Signal Via and GND Via

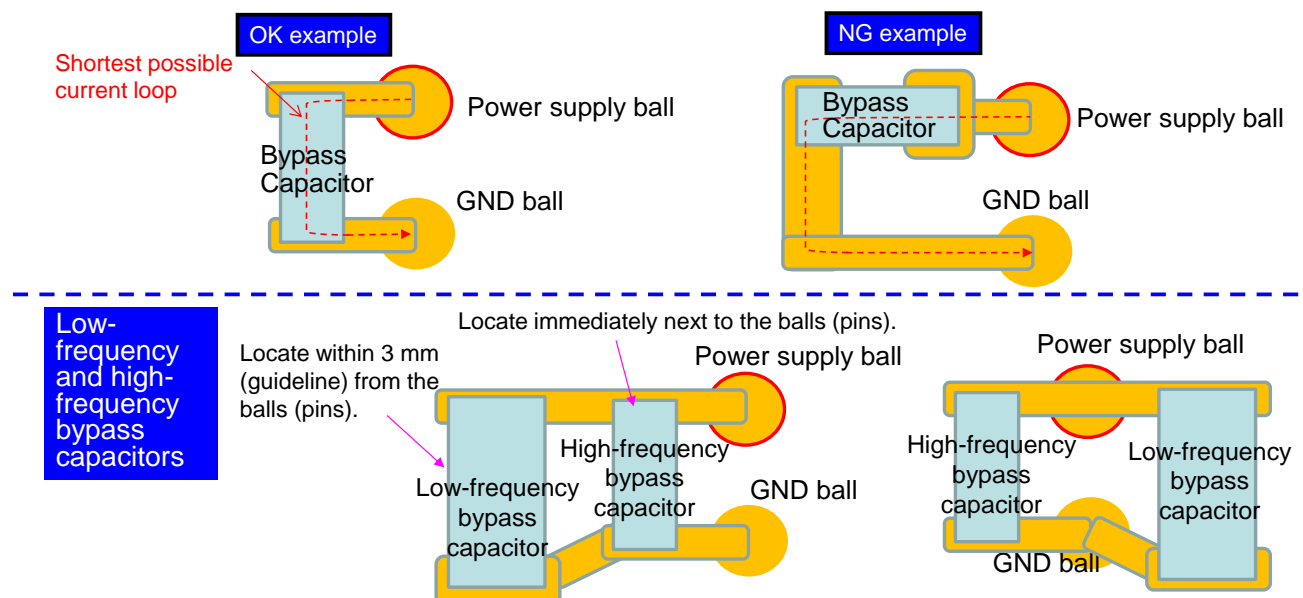
1. Signal Via and GND Via

When it is necessary to route a signal line to a different layer through a via, if at all possible arrange the signal via and GND via in a manner to avoid creating a stub. In the event that a stub is created, make sure that the stub length is within 1 mm (guideline).



3.4.4. SLVS-EC Power Supply Layout(Artwork)

1. SLVS-EC Power Supply Plane (I/F Power Supply; PLL Power Supply)
Perform the layout(artwork) on a solid surface.
2. GND Plane to be Secured for the Return Current Path
Perform the GND layout(artwork) using a solid surface.
Whether to provide a dedicated GND for each power supply or to use a shared GND of the solid surface is T.B.D.
3. Bypass Capacitor Placement
Locate the SLVS-EC power supply bypass capacitors immediately next to the sensor.
Make the routing as short as possible, including the return current path.
Locate the SLVS-EC power supply bypass capacitors immediately next to the balls (pins).
(The bypass capacitors are assumed to be located on the opposite side of the sensor.)
Make the routing as short as possible, including the return current path.



3.4.5. INCK

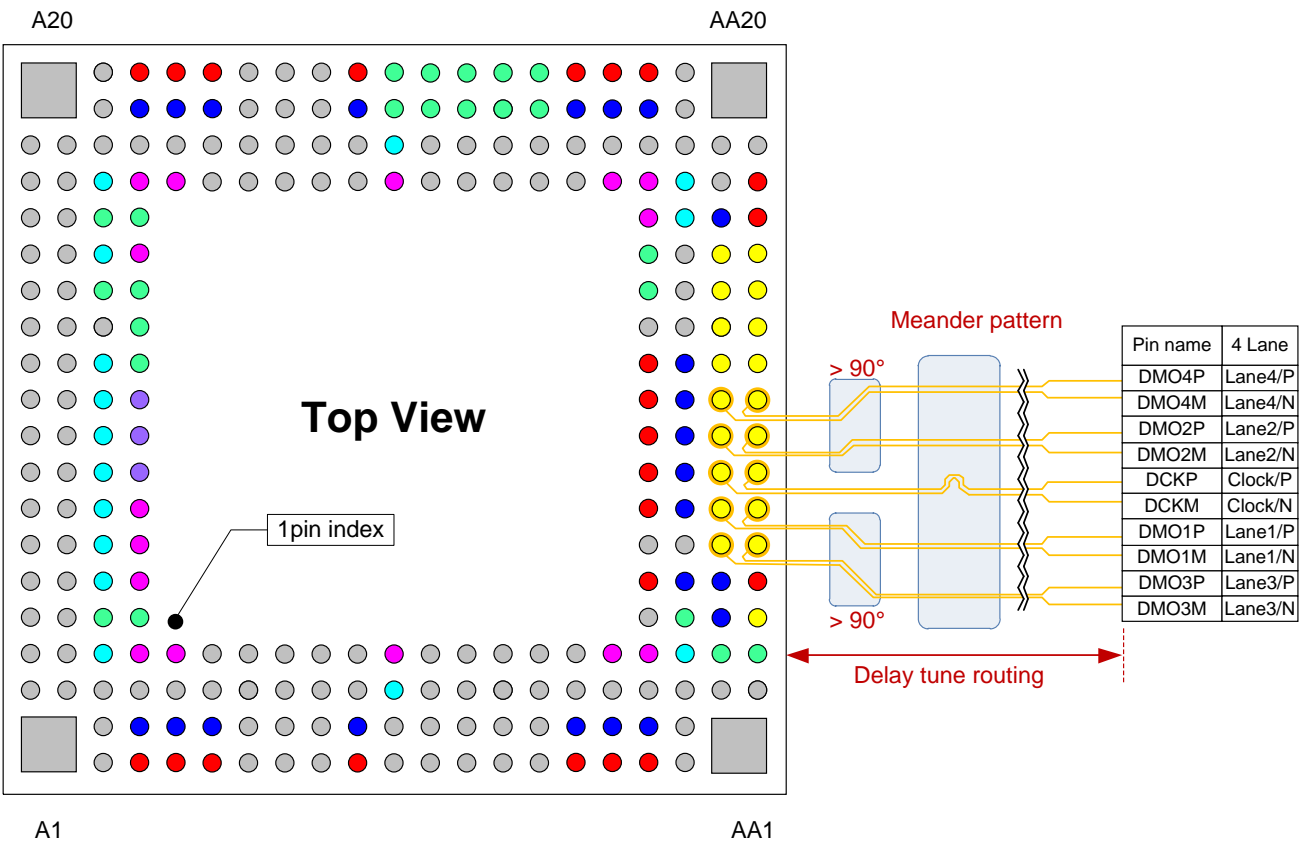
1. Routing
Use the routing layout that results in the shortest routing possible.
The Ref GND should be a solid GND.
Arrange the routing so that there is no crosstalk between analog power supplies, signals and INCK.
Separate routing by 3 times or more the width of the signal lines or shield with GND to prevent signal lines from running parallel with other routing.

3.5. CSI-2 serial Output

IMX294 is supported outout formart CSI-2. This section described about wiring pattern for CSI-2 output.

3.5.1 Wiring patterns for CSI-2 serial Output

1. Signal wires (DMOxP and DMOxM, DCKP and DCKM) must be paired. (Differential impedance is 100 Ω typ.)
2. We recommend delay tune wiring for image signals, especially delay of each differential pair signal and Data and its Strobe signal should be controlled by using meander wiring. Turning point angle of the wire should be greater or equal to 90 degree. (Obtuse angle)
3. Decoupling capacitors for digital power supply (V_{DD1}) should be mounted close to the power supply pins of the package of the sensor with using small size (1005M or 0603M) laminated layer ceramic capacitor.



Example of Wiring Patterns for CSI-2 Serial Output Signal

4. SLVS-EC

This section describes the SLVS-EC overview supported by IMX294.

4.1. SLVS-EC overview

SLVS-EC embeds the clock to the stream of data.

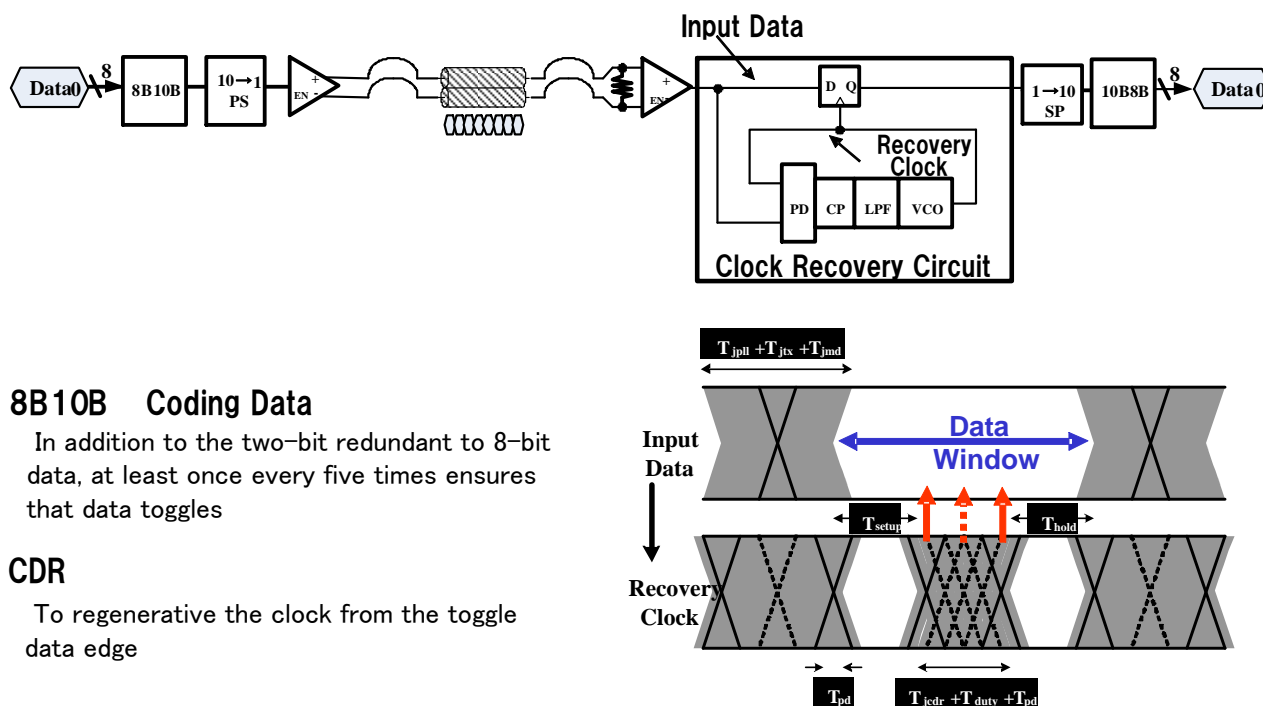
As a result it was made unnecessary the skew adjustment troubled by high-speed interface.

The outline / For further information of SLVS-EC standard, please refer the following document.

- SLVS-EC Specification Version 1.2

4.1.1. Embedded Clock

For embedding the clock in the data, skew adjustment is not required.



8B10B Coding Data

In addition to the two-bit redundant to 8-bit data, at least once every five times ensures that data toggles

CDR

To regenerative the clock from the toggle data edge

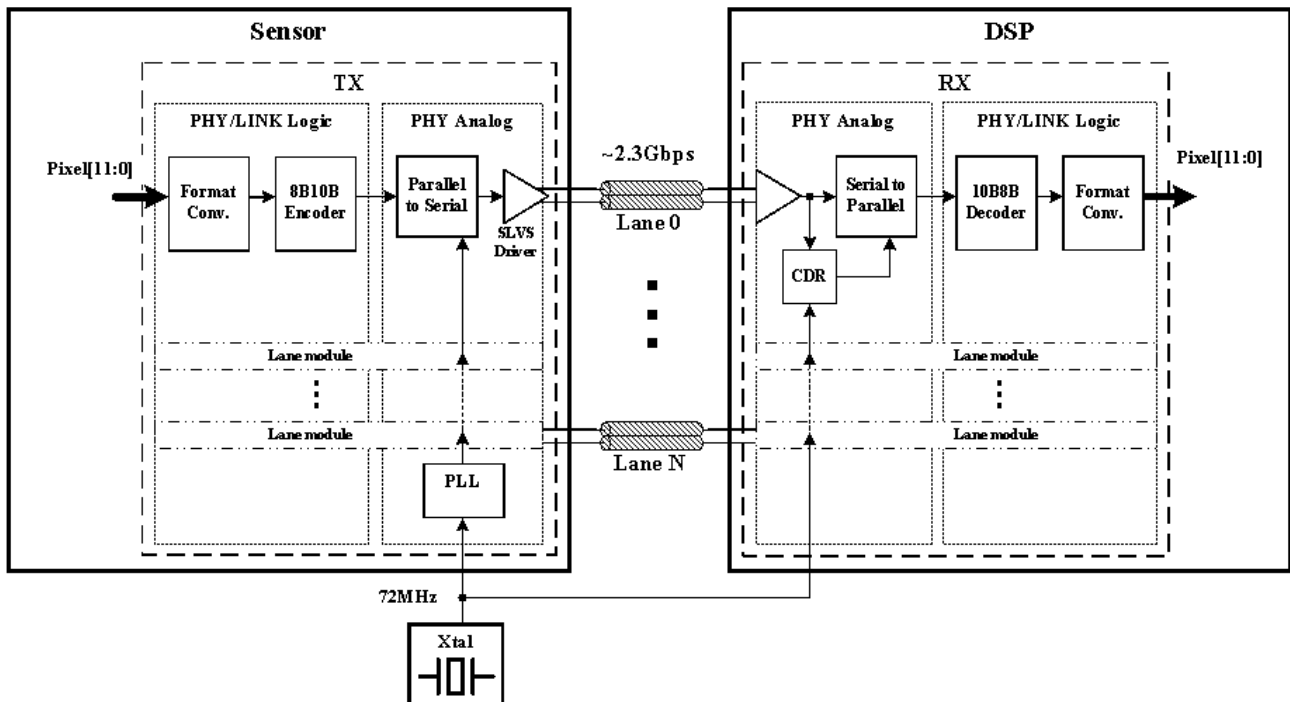
4.1.2. SLVS-EC Block chart

SLVS-EC block is composed of LINK Logic, PHY Logic, PHY Analog.

LINK Logic: To convert the pixel information in Byte units.

PHY Logic: To make the protocol control - 8B10B conversion and synchronization code addition.

The PHY Analog: To serialized and output in SLVS level.



5. MIPI

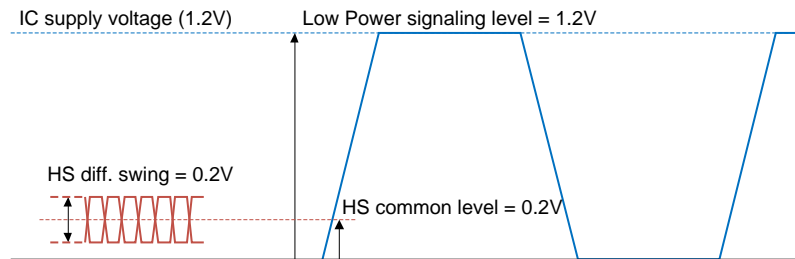
This section describes the operation of output mode supported by IMX294.

5.1. CSI-2 Serial Output

For details of MIPI Standard, output format, packet header and footer, please refer followings.

- MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

5.1.1. LANE states and Line Levels



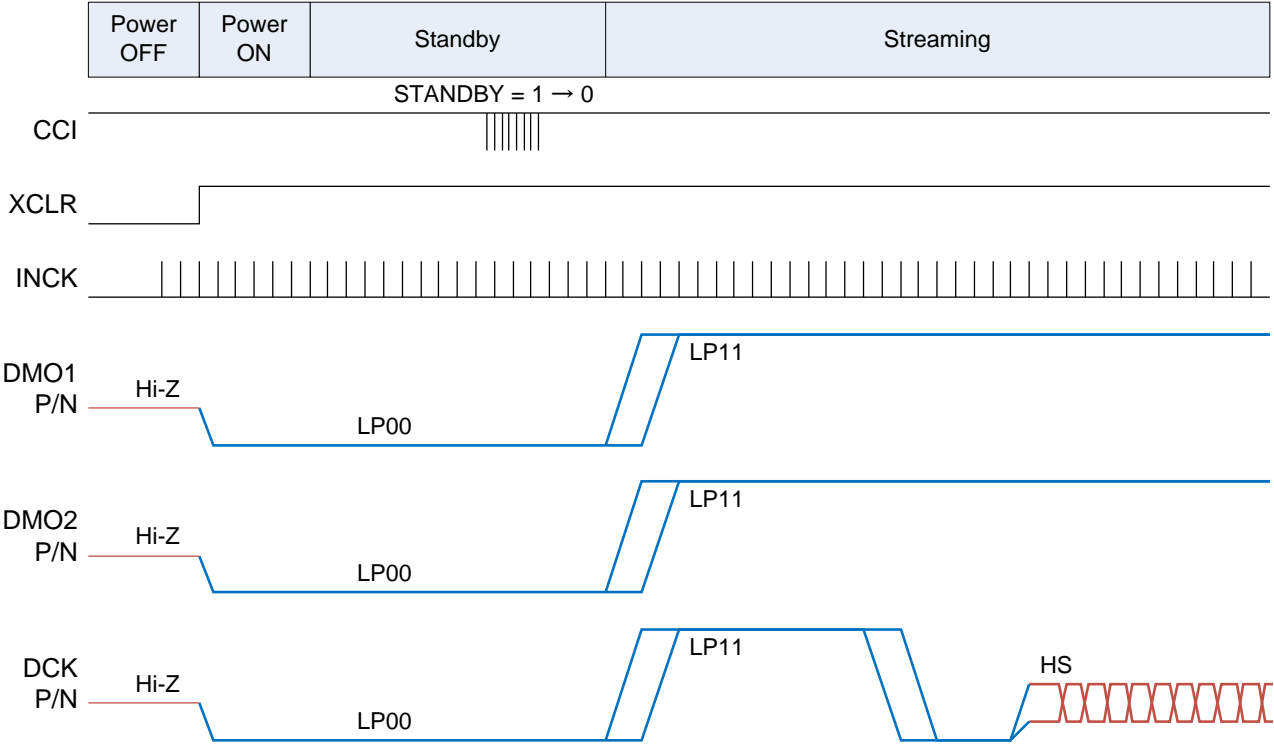
5.1.2. Turn-around mode

This sensor has no Turn-around mode function

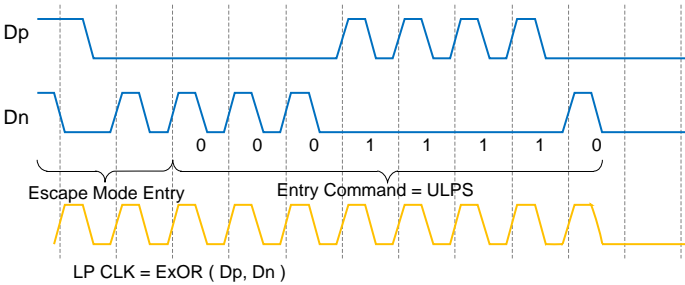
5.1.3. Escape mode

This sensor has Escape mode function. When the state is the followings, the sensor will change to ULPS after escape mode.

- ◆ Power On, Off
- ◆ Standby mode



Power On Sequence



ULPS (Ultra-Low Power State) command in Escape Mode

5.1.4. DC Specification

HS mode

HS Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	
$\Delta V_{\text{CMTX}(1,0)}$	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	
V_{OD}	HS transmit differential voltage	140	200	270	mV	
ΔV_{OD}	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	10	mV	
V_{OHHS}	HS output high voltage	-	-	360	mV	
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch	-	-	10	%	

LP mode

LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transfer	110			Ω	

5.1.5. AC specification

HS mode

HS Transmitter AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta V_{\text{CMTX(HF)}}$	Common-level variations above 450 MHz	-	-	15	mV _{RMS}	
$\Delta V_{\text{CMTX(LF)}}$	Common-level variations between 50 - 450 MHz	-	-	25	mV _{PEAK}	
t_R and t_F	20% - 80% rise time and fall time	150	-	300	ps	
T_{skew}		- 0.15	-	0.15	ps	

LP mode

LP Transmitter AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
$T_{\text{RLP}} / T_{\text{FLP}}$	15% - 85% rise time and fall time	-	-	25	ns	
V_{OL}	Slew rate Max. @ $C_{\text{LOAD}} = 20$ pF	-	-	250	mV/ns	
	Slew rate Min. @ $C_{\text{LOAD}} = 0 - 70$ pF	30	-	-	mV/ns	
C_{LOAD}	Load capacitance	0	-	70	pF	

6. Serial Communication Port

IMX294 have the 3-wire serial communication and I²C communication. This section describes the operation of these serial interfaces.

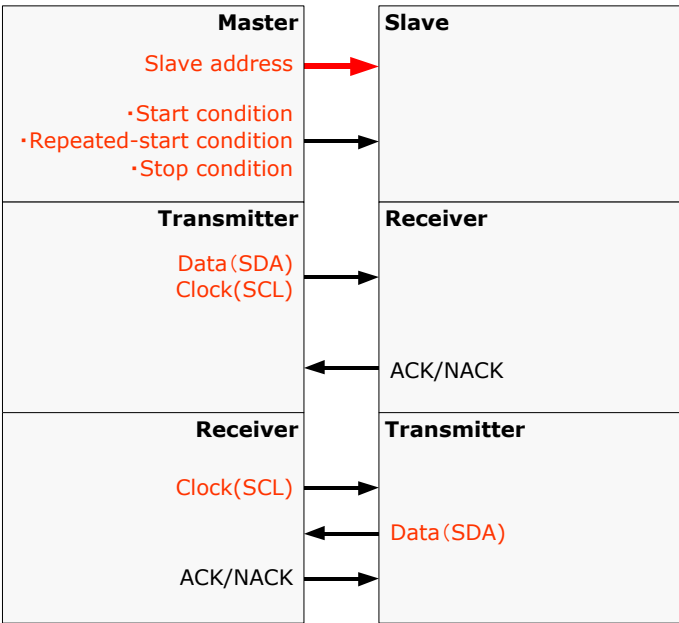
6.1. I²C Communication

- ◆ I²C consists of 2 wires of serial data and serial clock.
- ◆ Unit of the communication is 8bit (1byte), bi-directional communication. And in case of continuous communication, no limitation for the numbers of byte for the communications. (However, limited by communication period.) Acknowledge bit (ACK/NACK) is required at the end of communication.
- ◆ MSB first protocol
e.g.) When sending 28h MSB first: 0010 1000.
- ◆ While communication, the device transferring the data is the transmitter, and the device receiving the data is the receiver. The "slave" provides acknowledge bit.
- ◆ IMX294 is slave.

I²C Communication mode for IMX294

Mode	Communication speed	Correspondent
Standard mode	100 kbps	Available
Fast mode	400 kbps	Available
High speed mode	3.4 Mbps	N/A

Slave Address	Slave Address [7:1]	MSB							LSB
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Sensor Master / Slave mode common	1Ah	0	0	1	1	0	1	0	R/W

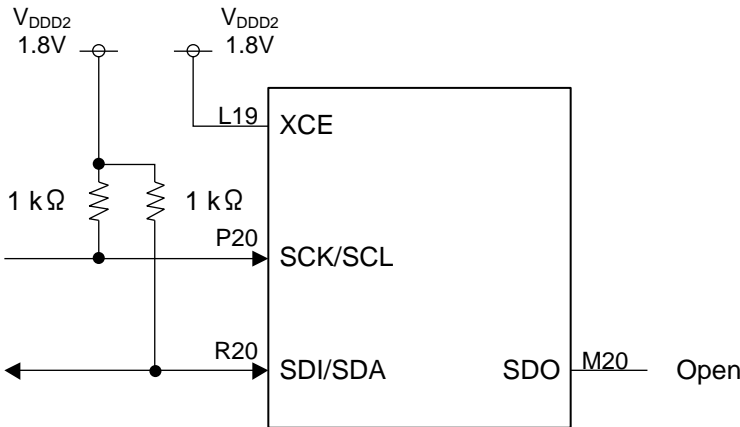


Relation between the sensor and the ISP when I²C communication

Master executes the following communication.

- ◆ Generate slave address (designed the device to be slave. Sensor is the slave here.)
- ◆ Generate “start condition”, “repeated start condition”, and “stop condition”.

While communication, the device transforming the data is the transmitter, and the device receiving the data is the receiver. Master can work as both transmitter and receiver, slave also work as both. Transmitter generates the data (SDA) and the clock (SCL), receiver generates the acknowledge Bit (ACK/NACK) and master always generates the clock (SCL) for acknowledge bit. Reference design for I²C serial communication is shown below. In addition, SCL, SDA, please pull up by 1kΩ to V_{DD2}.



Reference design for I²C serial communication

Overview of the communication protocol

Data is transferred by SDA port. The transition timing of the SDA follows the rule below.

- ◆ State control (start, restart, stop of the communication) is done while SCL is "high".
- ◆ When data transfer, SDA toggles while SCL is "low"

State control (start, restart, stop of the communication)

The conditions of start (start condition), restart (repeated start condition), and stop (stop condition) of the communication is shown below. State control is done by master device.

State condition	Condition
Start condition	SDA toggles from High to Low while SCL is high.
Repeated start condition	start condition while stop condition is of the previous data transfer is not generated
Stop condition	SDA toggles from Low to High while SCL is High.

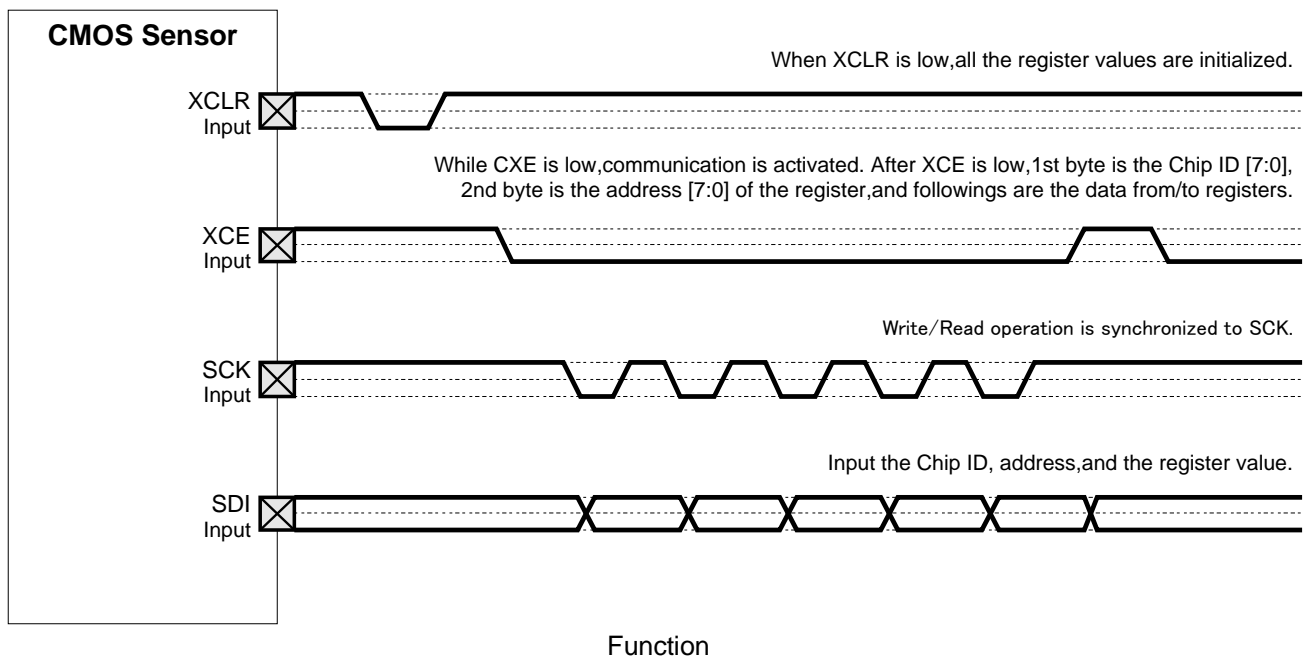
Acknowledge bit

Data transfer is done in unit of 8bit (1 byte). The acknowledge bit is generated for every 8bit data transfer and added after the last (8th) bit to indicate that receiver normally received the data. When receiver wants to stop the communication by the internal interrupt or etc. receiver generates the negative acknowledge bit (NACK).

- ◆ Master must send the slave address after declaration of the "Start condition" and "Repeated start condition".
- ◆ When slave generates the negative acknowledge bit, master declares the stop condition and stops the communication immediately.

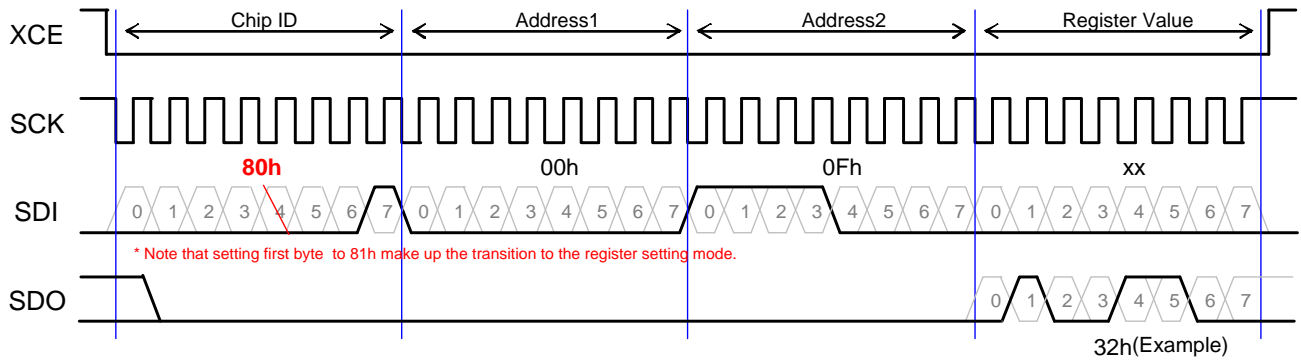
6.2. 3-wire Communication

- ◆ 3-wire serial interface consists of serial data input (SDI), serial clock (SCK), and chip enable (XCE). SDO is the data output port for read out the value in the registers.
- ◆ Data transfer is done in unit of 8bit (1byte). In case of continuous communication, no limitation for the numbers of byte for the communications. (However, limited by communication period.)
- ◆ LSB first protocol.
e.g.) When sending 8'h28 LSB first transfer is 0001 0100.



◆ Sony CIS can read the register value through SDO (test pin) for debugging purposes. Below is a concrete example of reading the value of address 000Fh by detecting SDO signal.

- Basically do the same way as normal register setting with the exception of the first byte. Set the first byte to the value other than ChipID(81h). Below is a example of setting to 80h.
- The 4th byte data of SDI pin is ignored and SDO pin outputs the register value of the specified address, which is synchronized with SCK's falling edge.



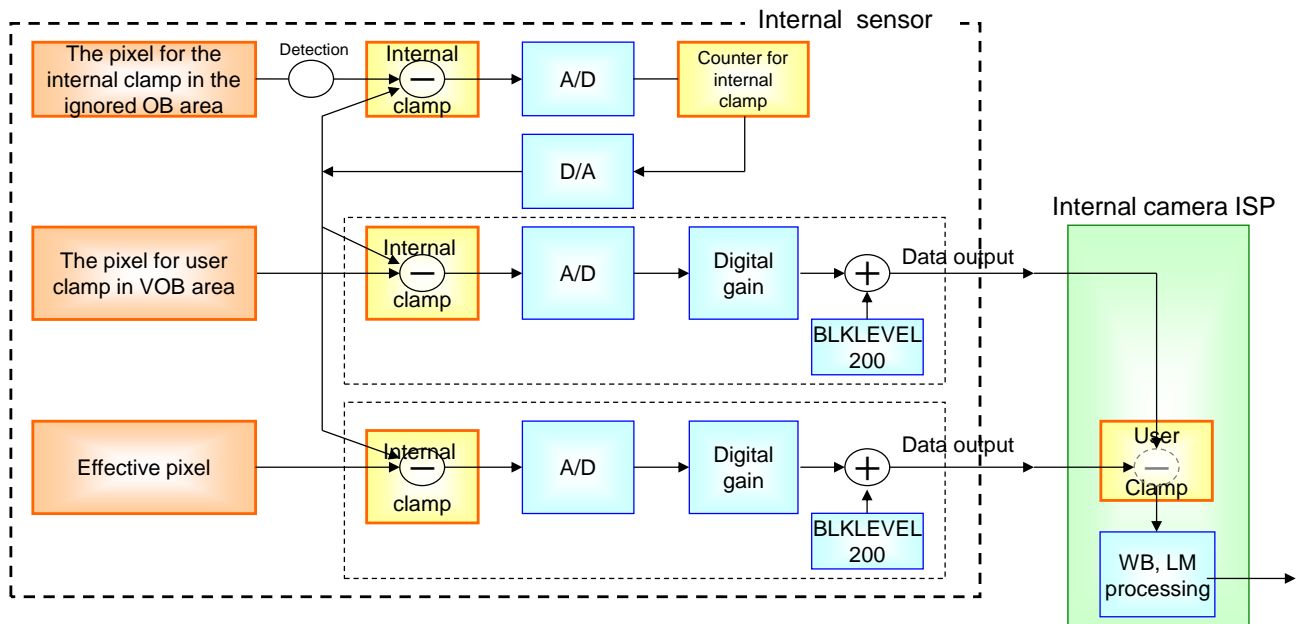
Read register value

7. Notes on clamp use

It will describe the precautions when using the clamp to be built into the IMX294.

7.1. Sensor Internal clamp and User clamp

- A rough internal clamp works in this sensor to secure the dynamic range of the AD converter movement.
- **Be sure to adopt the clamp function which uses VOB in the camera ISP** because black level may change by the noise under high gain.



Sensor Internal clamp and User clamp

8. Pattern Generator

This chapter explains the pattern generator (PG) function.

8.1. List of Pattern

- ◆ All 0000h Pattern
- ◆ All 3FFFh Pattern
- ◆ All 1555h Pattern
- ◆ All 2AAAh Pattern
- ◆ Horizontal Color-bar Chart
- ◆ Vertical Color-bar Chart

8.2. Register Map for Pattern Generator Function

The Register map for Pattern Generator is shown below.

Please refer to the datasheet for registers setup other than those lists.

Address		Bit assign-ment	Default value	Update timing	Name	Function	Remarks
CSI-2 (I ² C)	SLVS-EC						
303Ah	003Ah	[0]	0h	Immediately	TESTCLKEN_MIPI	Test mode clock control 0h:Stand-by 1h:Normal Set "1h" for using test pattern.	Range of setting value 0h to 1h For MIPI mode
		[1]	0h	Immediately	TESTCLKEN_EC	Test mode clock control 0h:Stand-by 1h:Normal Set "1h" for using test pattern.	Range of setting value 0h to 1h For SLVS-EC mode
		[3:2]	0h				Set default value.
		[4]	0h	Immediately	TESTPATEN	Test mode controlling 0h:Normal 1h:Test mode Set "1h" for using test pattern.	Range of setting value 0h to 1h
		[7:5]	0h				Set default value.
303Bh	003Bh	[4:0]	00h	Immediately	TESTPATSEL	Test pattern selecting 00h:ALL-000h Pattern 01h:ALL-FFFh Pattern 02h:ALL-555h Pattern 03h:ALL-AAAh Pattern 0Ah:Horizontal color bar 0Bh:Vertical color bar	Range of setting value 00h to 03h, 0Ah to 0Bh
		[7:5]	0h				Set default value.


Set the register as below when recovering the normal mode.

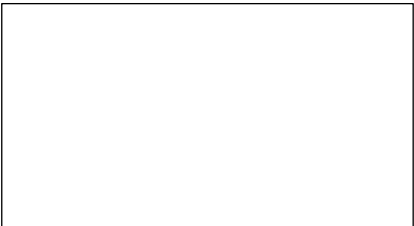
Address : 303Ah [7:0] Data : 00h , Address : 303Bh [7:0] Data : 00h (MIPI mode)


Address : 003Ah [7:0] Data : 00h , Address : 003Bh [7:0] Data : 00h (SLVS-EC mode)


8.3. List of Pattern

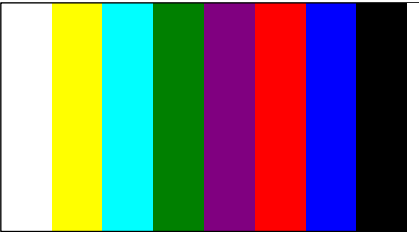
The pattern which it outputs by this function is shown below.
If set to register that is not described below, setting is invalid.

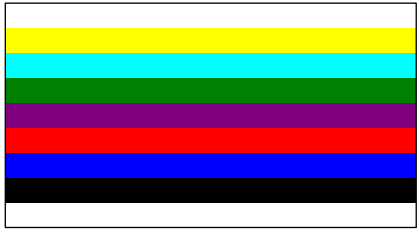
All 0000h Pattern		
Register	Pattern	Description
TESTPATSEL = 00h		All 0000h pattern

All 3FFFh Pattern		
Register	Pattern	Description
TESTPATSEL = 01h		All 3FFFh pattern 14bit: All 3FFFh 12bit: All FFFh 10bit: All 3FFh

All 1555h Pattern		
Register	Pattern	Description
TESTPATSEL = 02h		All 1555h pattern 14bit: All 1555h 12bit: All 555h 10bit: All 155h

All 2AAAh Pattern		
Register	Pattern	Description
TESTPATSEL = 03h		All 2AAAh pattern 14bit: All 2AAAh 12bit: All AAAh 10bit: All 2AAh

Horizontal Color-bar Chart		
Register	Pattern	Description
TESTPATSEL = 0Ah		Outputs the color bar which changes horizontally.

Vertical Color-bar Chart		
Register	Pattern	Description
TESTPATSEL = 0Bh		Outputs the color bar which changes vertically.

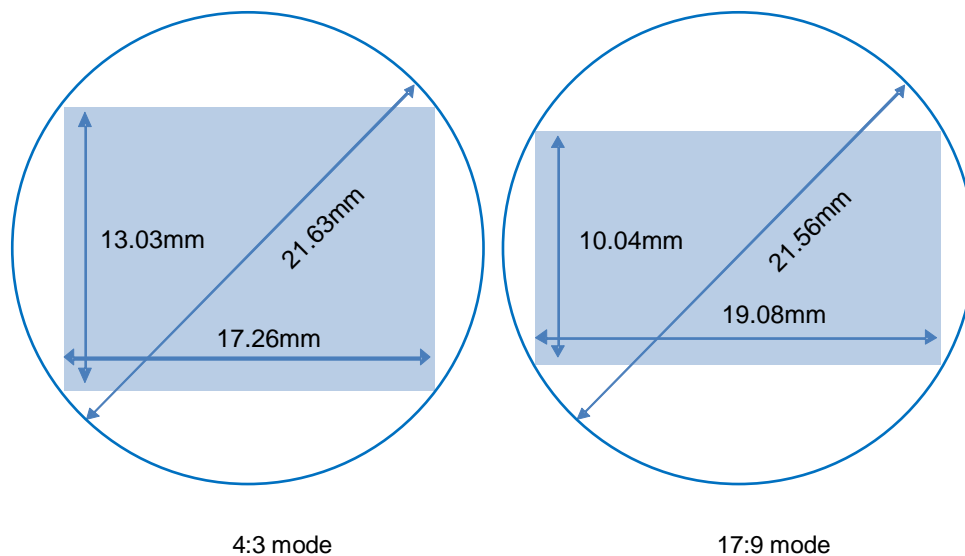
9. Lens Design Guideline

IMX294 have 4:3 scan mode and approx. 17:9 scan mode(Multi-Aspect).
This section describes the information to select the lens for this sensor.

9.1. Optical Dimension

- ◆ Image Size
 - 4:3 all-pixel scan mode : 21.63 mm (Type 4/3)
 - 17:9 all-pixel scan mode : 21.56 mm (Type 4/3)
- ◆ Number of active pixels
 - 4:3 all-pixel scan mode : 3728 (H) × 2814 (V) Approx. 10.49Mpixels
 - 17:9 all-pixel scan mode : 4120 (H) × 2168 (V) Approx. 8.93Mpixels
- ◆ Unit cell Size
 - 4.63 μm (H) × 4.63 μm (V)

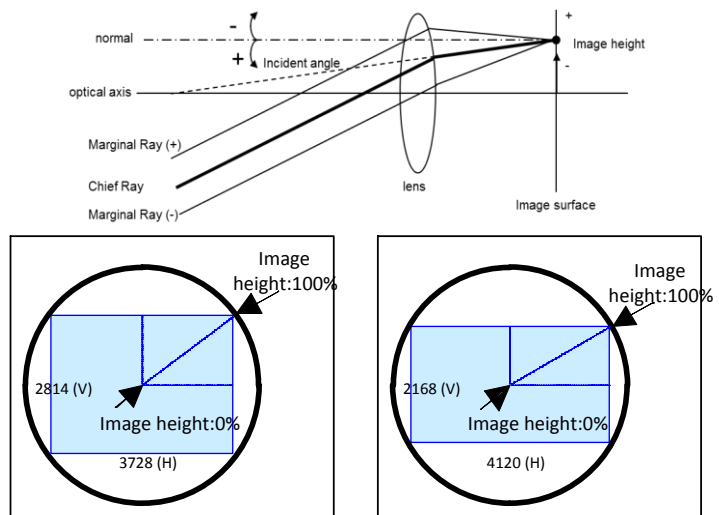
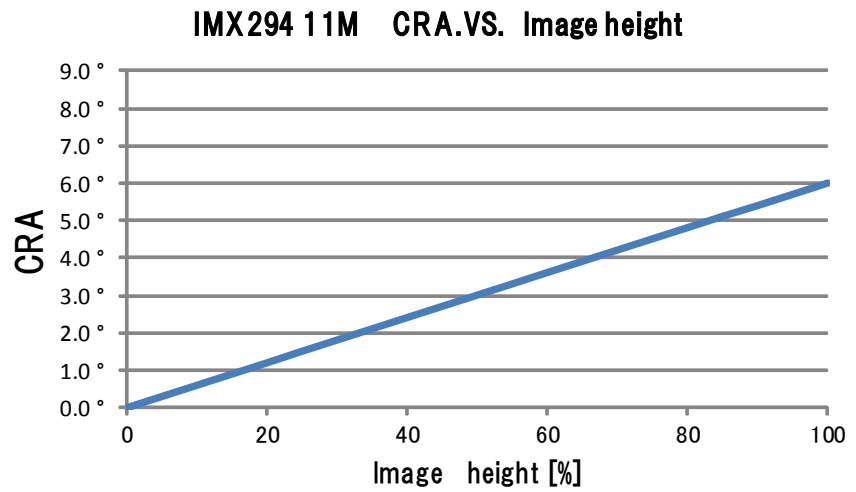
Image formation on IMX294 with the lens is shown below. Considering the color process (de-mosaic etc.) of the image, we recommend that the marginal area for color process is also inside of the image circle. (The necessary margin for color process depends on the algorithm of the de-mosaic. Please investigate the optimum number of the pixels.)



Relation between Image Circle and Pixel Area.

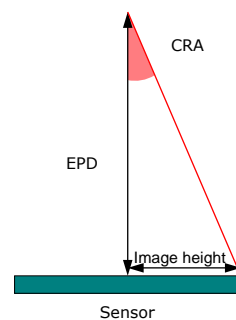
9.2. CRA Characteristics

Image Height		CRA
%	mm	deg
0	0.00 mm	0.0 °
5	0.54 mm	0.3 °
10	1.07 mm	0.6 °
15	1.61 mm	0.9 °
20	2.14 mm	1.2 °
25	2.68 mm	1.5 °
30	3.22 mm	1.8 °
35	3.75 mm	2.1 °
40	4.29 mm	2.4 °
45	4.82 mm	2.7 °
50	5.36 mm	3.0 °
55	5.90 mm	3.3 °
60	6.43 mm	3.6 °
65	6.97 mm	3.9 °
70	7.50 mm	4.2 °
75	8.04 mm	4.5 °
80	8.58 mm	4.8 °
85	9.11 mm	5.1 °
90	9.65 mm	5.4 °
95	10.18 mm	5.7 °
100	10.72 mm	6.0 °



About CRA Characteristics

CRA (Chief Ray Angle) indicates the optimum angle of the chief ray for the image height, independent from the aperture size of the lens.



CRA characteristics

10. FAQ

10.1. In case the image cannot be displayed with the finished sensor board

- ◆ Please confirm that the power supply design is according to the specification
 - Please confirm that the applied power supply voltage level is within the recommended range (Analog Power: typical value $\pm 0.1V$, Digital and Interface Power : typical value $\pm 0.1V$)
 - Please confirm that the power supply capacity is enough for the total current consumption requirement of the board including the sensor
 - Please confirm that the direction of the sensor (the foot print of the board and the chip) is correct
- ◆ Please make sure you have met the specifications of the standby release sequence of specification.

10.2. In case there is noise observed in the output image

- ◆ Vertical or horizontal stripes, always present
 - Please confirm that the decoupling capacitor of the power supply has sufficient capacitance and is put close to the sensor pin.
 - Please also confirm that the decoupling capacitor of VRLS, VRLT pin has sufficient capacitance as well.
- ◆ Horizontal stripes with random timing, often present
 - Please confirm that the register communication timing and the sensor data output timing are not overlapped. Conduct the register communication during the assigned period of the operation mode.
- ◆ Posterization, bit loss
 - Please confirm that the bit depth of the captured image data and that of the output image data are matched.
 - It is possible that the data capture timing is critical. Please compare the output waveform of the data out pin against that of the data clock pin to confirm that there is no problem with the data capture timing.

11. Revision History

Revision	Date	Page	Remarks
Rev.0.1	2016 /06/17	-	Tentative First edition