
Description

The IMX294CJK-C is a diagonal 21.63 mm (Type 4/3) CMOS image sensor with a color square pixel array and approximately 10.71 M effective pixels. 12-bit digital output makes it possible to output the signals of approximately 9.07 M effective pixels (approx. 17:9 aspect ratio) with high definition for moving pictures. It also operates with three power supply voltages: analog 2.9 V, digital 1.2 V, and 1.8 V for I/O interface and achieves low power consumption.

Furthermore, it realizes 12-bit digital output for shooting high-speed moving pictures by horizontal and vertical addition and subsampling. Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable storage time.

(Application: Surveillance, FA cameras, Industrial cameras)

Features

- ◆ CMOS active pixel type pixels
- ◆ Input clock frequency 6 to 27 MHz (CSI-2), 72 MHz (SLVS-EC)
- ◆ Both MIPI Specifications (CSI-2 high-speed serial interface) and SLVS-EC interface supported
- ◆ Multi-Aspect (approx. 17:9 and 4:3)
- ◆ All-pixel scan mode (approx. 17:9 and 4:3)
 - Horizontal/vertical 2/2-line binning mode (approx. 17:9 only)
 - Vertical 2 binning horizontal 2/4 subsampling mode (approx. 17:9 only)
 - Horizontal/vertical 2/4 subsampling mode (approx. 17:9 and 4:3)
 - Horizontal/vertical 3/3-line binning mode (approx. 17:9 only)
 - Vertical 1/3 subsampling horizontal 3 binning mode (approx. 17:9 only)
 - Vertical 2/9 subsampling binning horizontal 3 binning mode (approx. 17:9 and 4:3)
- ◆ High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- ◆ Vertical and horizontal arbitrary cropping function
- ◆ Variable-speed shutter function (minimum unit: 1 horizontal period)
- ◆ Low power consumption
- ◆ High dynamic range (HDR) function
- ◆ H driver, V driver and serial communication circuit on chip
- ◆ CDS/PGA on chip: Gain +27 dB (step pitch 0.1 dB)
- ◆ 10-bit/12-bit/14-bit A/D conversion on chip
- ◆ R, G, B primary color mosaic filters on chip (Quad Bayer structure)
- ◆ All-pixel simultaneous reset supported
- ◆ 248-pin high-precision ceramic package

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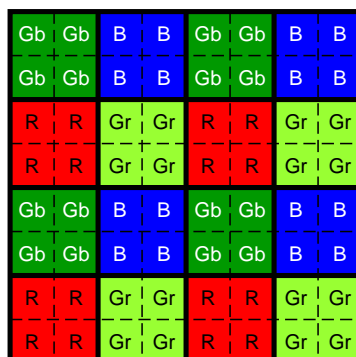
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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits.

Device Structure

◆ CMOS image sensor (Quad Bayer structure)

Quad Bayer structure is constructed of 4 same color pixels into which 1 pixel of bayer pixel array is divided as following figure.



Quad Bayer Structure

HDR function is available by dividing exposure time in the 4 same color pixels into long exposure pixels and short exposure pixels.

When normal operation, 4 same color pixels are added and made 1 pixel, and output as bayer pixel array.

In addition, a group of divided 4 same color pixels is defined as 1 pixel unit in this product specification.

◆ Image size

Diagonal 21.63 mm (Type 4/3) Multi-Aspect (Aspect ratio 4:3 and approx. 17:9)

◆ Total number of pixels

- Aspect ratio approx. 17:9 : 4200 (H) × 2184 (V) approx. 9.17 M pixels
- Aspect ratio 4:3 : 3840 (H) × 2840 (V) approx. 10.91 M pixels

◆ Number of effective pixels

- Aspect ratio approx. 17:9 : 4168 (H) × 2176 (V) approx. 9.07 M pixels
- Aspect ratio 4:3 : 3792 (H) × 2824 (V) approx. 10.71 M pixels

◆ Number of active pixels

- Aspect ratio approx. 17:9 : 4120 (H) × 2168 (V) approx. 8.93 M pixels diagonal 21.56 mm
- Aspect ratio 4:3 : 3728 (H) × 2814 (V) approx. 10.49 M pixels diagonal 21.63 mm

◆ Number of recommended recording pixels

- Aspect ratio approx. 17:9 : 4096 (H) × 2160 (V) approx. 8.85 M pixels
- Aspect ratio 4:3 : 3704 (H) × 2778 (V) approx. 10.29 M pixels

◆ Chip size

24.553 mm (H) × 20.013 mm (V) (include scribe area)

◆ Unit cell size

4.63 μm (H) × 4.63 μm (V)

◆ Optical black

Horizontal (H) direction : Front 0 pixel, rear 0 pixel

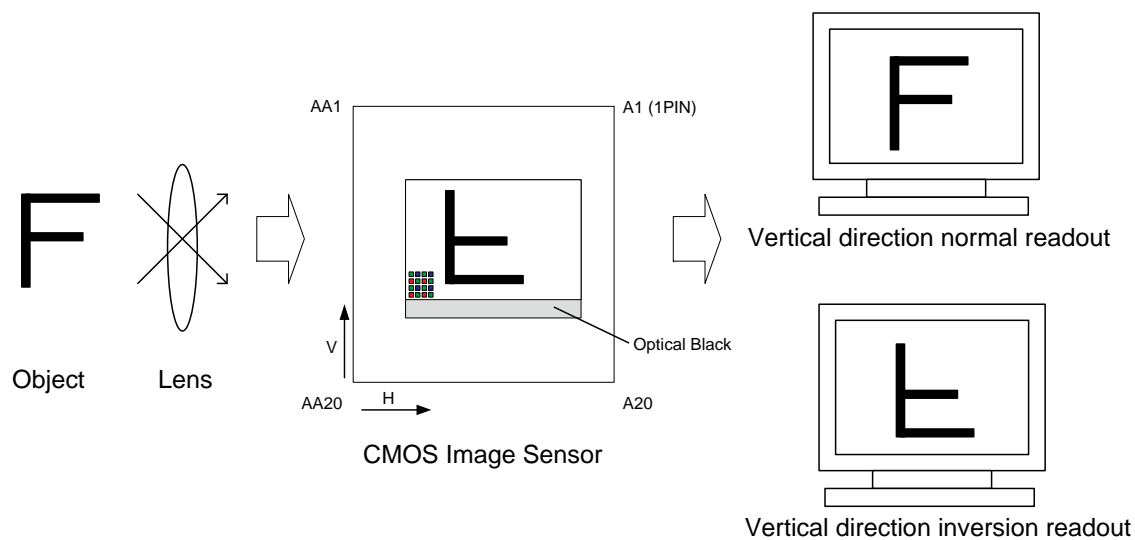
Vertical (V) direction : Front 16 pixels, rear 0 pixel

◆ Substrate material

Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Optical Black Array and Readout Scan Direction

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage (Analog)	V _{ADD} ^{*1}	−0.3 to +3.3	V
Supply voltage (Digital 1)	V _{DD1} ^{*2}	−0.5 to +2.0	V
Supply voltage (Digital 2)	V _{DD2} ^{*3}	−0.5 to +3.3	V
Supply voltage (Digital 3)	V _{DD3} ^{*4}	−0.5 to +2.0	V
Input voltage (Digital)	V _I	−0.3 to V _{DD2} + 0.3	V
Output voltage (Digital)	V _O	−0.3 to V _{DD2} + 0.3	V
Guaranteed operating temperature	T _{OPR}	−10 to +75	°C
Storage guarantee temperature	T _{STG}	−30 to +80	°C
Performance guarantee temperature	T _{SPEC}	−10 to +60	°C

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Supply voltage (Analog)	V _{ADD} ^{*1}	2.9 ± 0.1	V
Supply voltage (Digital 1)	V _{DD1} ^{*2}	1.2 ± 0.1	V
Supply voltage (Digital 2)	V _{DD2} ^{*3}	1.8 ± 0.1	V
Supply voltage (Digital 3)	V _{DD3} ^{*4}	1.2 ± 0.1	V
Input voltage (Digital)	V _I	−0.1 to V _{DD2} + 0.1	V

^{*1} V_{ADD}: V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP (2.9 V power supply)

^{*2} V_{DD1}: V_{DD}LCN, V_{DD}LCM, V_{DD}LSC, V_{DD}LSA, V_{DD}LPL (1.2 V power supply)

^{*3} V_{DD2}: V_{DD}MIO, V_{DD}MPX (1.8 V power supply)

^{*4} V_{DD3}: V_{DD}LPLA, V_{DD}LPLD, V_{DD}LIF (1.2 V power supply)

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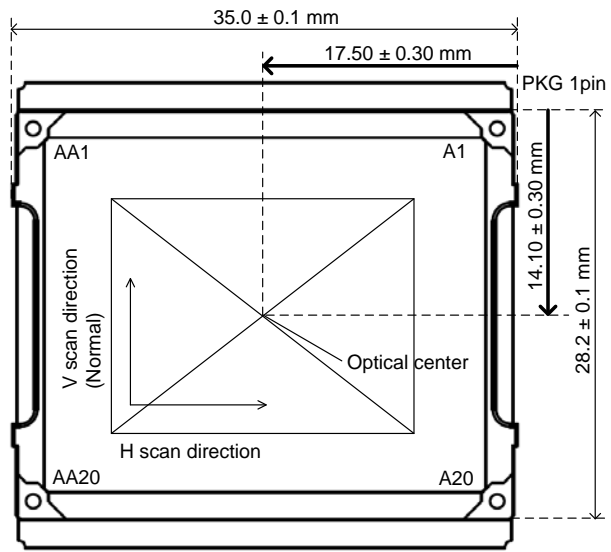
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Optical Center

(Top View)



* See page 155 “Package Outline” for details

Optical Center

Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	
20	NC_6		NC_6	VssLSC	VssLCM	VssLCN	NC_8	NC_8	NC_8	VssLSC	XVS	SDO	XHS	SKK /SOL	SDI /SDA	VssLCN	VssLCM	VssLSA	NC_13	NC_13		20
19			NC_6	VssLSC	VssLCM	VssLCN	NC_8	NC_8	NC_8	VssLSC	XGE	TEST3	TEST4	XCLR	TEST5	VssLCN	VssLCM	VssLSA	NC_13			19
18	NC_5	NC_5	NC_5	NC_5	NC_5	NC_5	NC_5	NC_5	NC_5	NC_5	VssHCM	NC_11	NC_11	NC_11	NC_11	NC_11	NC_11	NC_11	NC_11	NC_11	NC_11	18
17	NC_4	NC_4	VssHPX	VssHPX	VssSUB	NC_5	NC_5	NC_5	NC_5	NC_5	VssHCM	NC_11	NC_11	NC_11	NC_11	NC_11	VssSUB	VssHPX	VssHPX	NC_11	VssMIO	17
16	NC_4	NC_4	VLOAD CMSF	VLOADLM														VssHDA	VssHDA	VssLSC	VssLSC	16
15	NC_4	NC_4	VssHPX	VssMPX														VBGR1	NC_11	DOM7	DOP7	15
14	NC_4	NC_4	VBGR2	TEST2														VEXRES1	NC_11	DOM6	DOP6	14
13	NC_4	NC_4	NC_4	VEXRES2														NC_11	NC_11	DOM5	DOP5	13
12	NC_4	NC_4	VssHPX	TEST1														VssLIF	VssLIF	DOM4	DOP4	12
11	NC_4	NC_4	VssHPX	VRLT														VssLIF	VssLIF	DOM3 /DMO4M	DOP3 /DMO4P	11
10	NC_3	NC_3	VssHPX	VRLS														VssLIF	VssLIF	DOM2 /DMO2M	DOP2 /DMO2P	10
9	NC_3	NC_3	VssHPX	VRLT_RD														VssLPLA	VssLPLA	DKM	DCKP	9
8	NC_3	NC_3	VssHDA	VssHDA														VssLPLD	VssLPLD	DOM1 /DMO1M	DOP1 /DMO1P	8
7	NC_3	NC_3	VssHCP	VssHCP														NC_10	NC_10	DOM0 /DMO3M	DOP0 /DMO3P	7
6	NC_3	NC_3	VssHPX	VssMPX														VssLPL	VssLPL	VssLSC	VssLSC	6
5	NC_3	NC_3	VLOAD CMSF	VLOADLM														NC_10	SLASEL	VssLPLD	INCK	5
4	NC_3	NC_3	VssHPX	VssHPX	VssSUB	NC_2	NC_2	NC_2	NC_2	NC_2	VssHCM	NC_10	NC_10	NC_10	NC_10	NC_10	VssSUB	VssHPX	VssHPX	TEST6	TEST7	4
3	NC_2	NC_2	NC_2	NC_2	NC_2	NC_2	NC_2	NC_2	NC_2	NC_2	VssHCM	NC_10	NC_10	NC_10	NC_10	NC_10	NC_10	NC_10	NC_10	NC_10	NC_10	3
2	NC_1		NC_1	VssLSC	VssLCM	VssLCN	NC_7	NC_7	NC_7	VssLSC	NC_9	NC_9	NC_9	NC_9	NC_9	VssLCN	VssLCM	VssLSA	NC_12	NC_12		2
1			NC_1	VssLSC	VssLCM	VssLCN	NC_7	NC_7	NC_7	VssLSC	NC_9	NC_9	NC_9	NC_9	NC_9	VssLCN	VssLCM	VssLSA	NC_12			1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	

The pin whose name is changed by which using CSI-2 or SLVS-EC is assigned both names.
NC pins whose NC_** number is same are connected in the package.

Pin Configuration

Pin Description

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
C4	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C5	VLOADCMSF	O	A	Capacitor connection		
C6	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C7	V _{SS} HCP	GND	A	Analog GND (2.9 V)	—	
C8	V _{SS} HDA	GND	A	Analog GND (2.9 V)	—	
C9	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C10	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C11	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C12	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C14	VBGR2	O	A	Capacitor connection		
C15	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
C16	VLOADCMSF	O	A	Capacitor connection		
C17	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
D1	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
D2	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
D4	V _{DD} HPX	Power	A	Analog power supply (2.9 V)	—	
D5	VLOADLM	O	A	Capacitor connection		
D6	V _{DD} MPX	Power	D	(Digital power supply (1.8 V))	—	Leave open. (No connection)
D7	V _{DD} HCP	Power	A	Analog power supply (2.9 V)	—	
D8	V _{DD} HDA	Power	A	Analog power supply (2.9 V)	—	
D9	VRLT_RD	O	A	Capacitor connection	Pull-down	
D10	VRLS	O	A	Capacitor connection	Pull-down	
D11	VRLT	O	A	Capacitor connection	Pull-down	
D12	TEST1	O	A	Test	Hi-Z	Leave open. (No connection)
D13	VEXRES2	O	A	Resister connection	Hi-Z	
D14	TEST2	O	A	Test	Hi-Z	Leave open. (No connection)
D15	V _{DD} MPX	Power	D	(Digital power supply (1.8 V))	—	Leave open. (No connection)
D16	VLOADLM	O	A	Capacitor connection		
D17	V _{DD} HPX	Power	A	Analog power supply (2.9 V)	—	
D19	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
D20	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
E1	V _{DD} LCM	Power	D	Digital power supply (1.2 V)	—	
E2	V _{SS} LCM	GND	D	Digital GND (1.2 V)	—	
E4	V _{DD} SUB	Power	A	Analog power supply (2.9 V)	—	
E17	V _{DD} SUB	Power	A	Analog power supply (2.9 V)	—	
E19	V _{SS} LCM	GND	D	Digital GND (1.2 V)	—	
E20	V _{DD} LCM	Power	D	Digital power supply (1.2 V)	—	
F1	V _{DD} LCN	Power	D	Digital power supply (1.2 V)	—	
F2	V _{SS} LCN	GND	D	Digital GND (1.2 V)	—	
F19	V _{SS} LCN	GND	D	Digital GND (1.2 V)	—	
F20	V _{DD} LCN	Power	D	Digital power supply (1.2 V)	—	
K1	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
K2	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
K19	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
K20	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
L3	V _{SS} HCM	GND	A	Analog GND (2.9 V)	—	
L4	V _{DD} HCM	Power	A	Analog power supply (2.9 V)	—	
L17	V _{DD} HCM	Power	A	Analog power supply (2.9 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
L18	V _{SS} HCM	GND	A	Analog GND (2.9 V)	—	
L19	XCE	I	D	Serial communication enable input	—	When using SLVS-EC
				Connect to 1.8 V power supply	—	When using CSI-2
		I	D	Vertical sync signal input	—	When using SLVS-EC
L20	XVS	O	D	Vertical sync signal output	—	When using CSI-2 If unused XVS, leave open.
M19	TEST3	I	D	Test	Pull-down	Leave open. (No connection)
M20	SDO	O	D	Test output	Low Level	Leave open. (No connection)
N19	TEST4	I	D	Test	—	Leave open. (No connection)
		I	D	Horizontal sync signal input	—	When using SLVS-EC
N20	XHS	O	D	Horizontal sync signal output	—	When using CSI-2 If unused XHS, leave open.
P19	XCLR	I	D	Reset pulse input	—	
P20	SCK	I	D	Serial communication clock input	—	When using SLVS-EC
	SCL	I	D	I ² C communication clock input	—	When using CSI-2
R19	TEST5	O	D	TEST	Low Level	Leave open. (No connection)
	SDI	I	D	Serial communication data input	—	When using SLVS-EC
R20	SDA	I/O	D	I ² C communication data input/output	—	When using CSI-2
T1	V _{DD} LCN	Power	D	Digital power supply (1.2 V)	—	
T2	V _{SS} LCN	GND	D	Digital GND (1.2 V)	—	
T19	V _{SS} LCN	GND	D	Digital GND (1.2 V)	—	
T20	V _{DD} LCN	Power	D	Digital power supply (1.2 V)	—	
U1	V _{DD} LCM	Power	D	Digital power supply (1.2 V)	—	
U2	V _{SS} LCM	GND	D	Digital GND (1.2 V)	—	
U4	V _{DD} SUB	Power	A	Analog power supply (2.9 V)	—	
U17	V _{DD} SUB	Power	A	Analog power supply (2.9 V)	—	
U19	V _{SS} LCM	GND	D	Digital GND (1.2 V)	—	
U20	V _{DD} LCM	Power	D	Digital power supply (1.2 V)	—	
V1	V _{DD} LSA	Power	D	Digital power supply (1.2 V)	—	
V2	V _{SS} LSA	GND	D	Digital GND (1.2 V)	—	
V4	V _{DD} HPX	Power	A	Analog power supply (2.9 V)	—	
V6	V _{DD} LPL	Power	D	Digital power supply (1.2 V)	—	
V8	V _{DD} LPLD	Power	D	Digital power supply (1.2 V)	—	
V9	V _{DD} LPLA	Power	D	Digital power supply (1.2 V)	—	
V10	V _{DD} LIF	Power	D	Digital power supply (1.2 V)	—	
V11	V _{DD} LIF	Power	D	Digital power supply (1.2 V)	—	
V12	V _{DD} LIF	Power	D	Digital power supply (1.2 V)	—	
V14	VEXRES1	O	A	Resister connection	Hi-Z	
V15	VBGR1	O	A	Capacitor connection	Hi-Z	
V16	V _{DD} HDA	Power	A	Analog power supply (2.9 V)	—	
V17	V _{DD} HPX	Power	A	Analog power supply (2.9 V)	—	
V19	V _{SS} LSA	GND	D	Digital GND (1.2 V)	—	
V20	V _{DD} LSA	Power	D	Digital power supply (1.2 V)	—	
W4	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
W5	SLASEL	I	D	(Pin for I ² C communication)	—	When using SLVS-EC Leave open. (No connection)
				Slave address control	Pull-up	When using CSI-2
W6	V _{SS} LPL	GND	D	Digital GND (1.2 V)	—	
W8	V _{SS} LPLD	GND	D	Digital GND (1.2 V)	—	
W9	V _{SS} LPLA	GND	D	Digital GND (1.2 V)	—	
W10	V _{SS} LIF	GND	D	Digital GND (1.2 V)	—	
W11	V _{SS} LIF	GND	D	Digital GND (1.2 V)	—	
W12	V _{SS} LIF	GND	D	Digital GND (1.2 V)	—	
W16	V _{SS} HDA	GND	A	Analog GND (2.9 V)	—	
W17	V _{SS} HPX	GND	A	Analog GND (2.9 V)	—	
Y4	TEST6	O	D	Test	Low Level	Leave open. (No connection)
Y5	V _{SS} LPLD	GND	D	Digital GND (1.2 V)	—	
Y6	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
Y7	DOM0	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO3M	O	D	Digital MIPI output	Low Level	When using CSI-2 Data Lane 3 connection
Y8	DOM1	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO1M	O	D	Digital MIPI output	Low Level	When using CSI-2 Data Lane 1 connection
Y9	DCKM	O	D	(Pin for CSI-2)		When using SLVS-EC Leave open. (No connection)
				Digital MIPI output	Low Level	When using CSI-2 Clock Lane connection
Y10	DOM2	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO2M	O	D	Digital MIPI output	Low Level	When using CSI-2 Data Lane 2 connection
Y11	DOM3	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO4M	O	D	Digital MIPI output	Low Level	When using CSI-2 Data Lane 4 connection
Y12	DOM4	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
Y13	DOM5	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
Y14	DOM6	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
Y15	DOM7	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
Y16	V _{SS} LSC	GND	D	Digital GND (1.2 V)	—	
AA4	TEST7	O	D	Test	Low Level	Leave open. (No connection)
AA5	INCK	I	D	Input clock	—	
AA6	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
AA7	DOP0	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO3P	O	D	Digital MIPI output	Low Level	When using CSI-2 For Data Lane 3
AA8	DOP1	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO1P	O	D	Digital MIPI output	Low Level	When using CSI-2 For Data Lane 1
AA9	DCKP	O	D	(Pin for CSI-2)		When using SLVS-EC Leave open. (No connection)
				Digital MIPI output	Low Level	When using CSI-2 For Clock Lane
AA10	DOP2	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO2P	O	D	Digital MIPI output	Low Level	When using CSI-2 For Data Lane 2
AA11	DOP3	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
	DMO4P	O	D	Digital MIPI output	Low Level	When using CSI-2 For Data Lane 4
AA12	DOP4	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
AA13	DOP5	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
AA14	DOP6	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
AA15	DOP7	O	D	Digital SLVS-EC output	Hi-Z	When using SLVS-EC
				(Pin for SLVS-EC)		When using CSI-2 Leave open. (No connection)
AA16	V _{DD} LSC	Power	D	Digital power supply (1.2 V)	—	
AA17	V _{DD} MIO	Power	D	Digital power supply (1.8 V)	—	

I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
$V_{DD}LSC$ $V_{DD}MIO$ $V_{DD}SUB$	
$V_{SS}LSC$	<p>$V_{SS}LSC1$ and $V_{SS}LSC2$ are internally connected.</p>
$V_{DDL}CN$	
$V_{SS}L CN$	
$V_{DDL}PL$	
$V_{SS}L PL$	
$V_{DDL}PLA$	
$V_{SS}L PLA$ $V_{SS}L PLD$	

□ External pins

Symbol	Equivalent circuit
$V_{DD}LPLD$	
V_{DDLIF}	
V_{SSLIF}	<p>V_{DDLIF}</p> <p>V_{SSLIF1} and V_{SSLIF2} are internally connected.</p>
$V_{DD}HPX$ $V_{DD}MPX$	
$V_{SS}HPX$	<p>V_{DDLCM} $V_{DD}HPX$ $V_{DD}HCM$</p>
$V_{DD}HCM$	
$V_{SS}HCM$	<p>$V_{DD}HPX$ $V_{DD}HCM$</p>
$V_{DD}HDA$	
$V_{SS}HDA$	<p>$V_{DD}HDA$</p>

□ External pins

Symbol	Equivalent circuit
V_{DDHCP}	
V_{SSHCP}	
V_{DDLCM}	
V_{SSLCM}	
V_{DDLSA}	
V_{SSLSA}	
VRLT VRLT_RD VRLS	
INCK XCE	

□ External pins


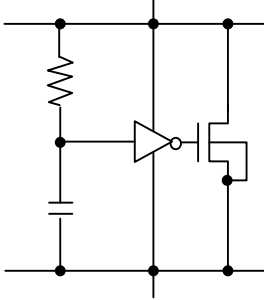
Symbol	Equivalent circuit
XVS XHS	
SDI/SDA SCK/SCL	
SLASEL	
XCLR	

□ External pins

Symbol	Equivalent circuit
VEXRES1 VEXRES2 VBGR1 VBGR2	
VLOADLM VLOADCMSF	
DMOxP DMOxM (x = 1 to 4) DCKP DCKM	
DOPx DOMx (x = 0 to 7)	

□ External pins

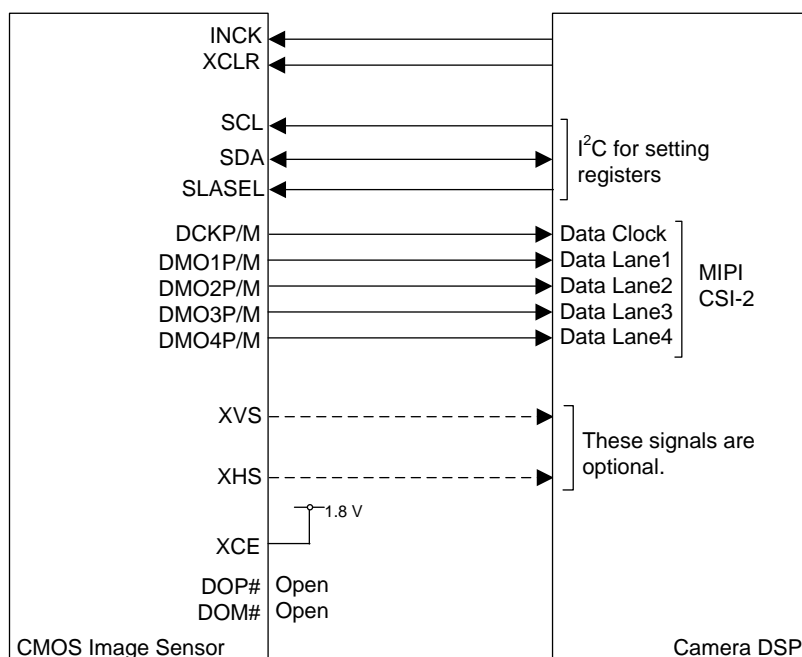
Description of Special Symbol

Symbol	Equivalent circuit
	

[illegible]

System Outline

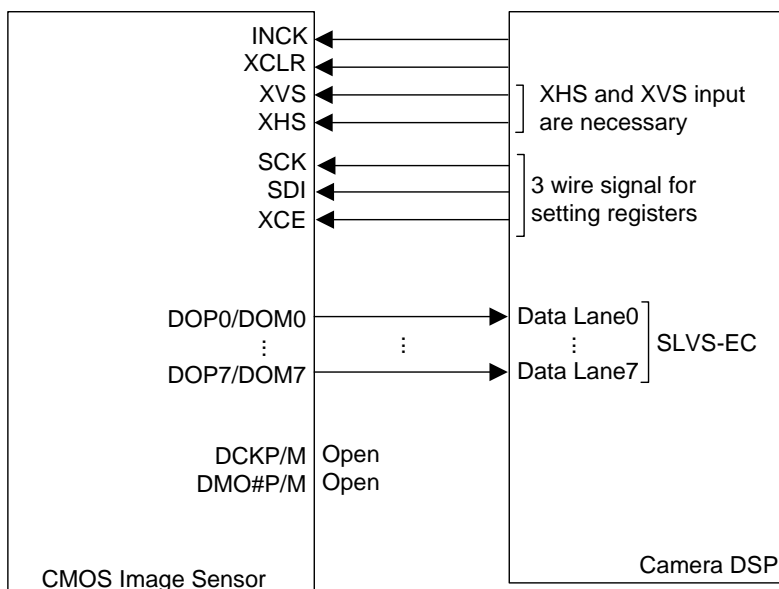
When using CSI-2



* I²C communication only can be used when using MIPI CSI-2

System Outline When Using CSI-2

When using SLVS-EC



* 3-wire serial communication only can be used when using SLVS-EC

* Sensor Slave operation only

System Outline When Using SLVS-EC

Electrical Characteristics when using CSI-2

1. DC Characteristics (CSI-2)

Current Consumption and Gain Variable Range (CSI-2)

($V_{ADD} = 3.0\text{ V}$, $V_{DDD1} = 1.3\text{ V}$, $V_{DDD2} = 1.9\text{ V}$, $V_{DDD3} = 1.3\text{ V}$, $T_j = 60\text{ }^{\circ}\text{C}$, Reference Gain (0 dB)
Aspect ratio 4:3, mode0(All pixel scan mode, AD 14bit), 24 frame/s)

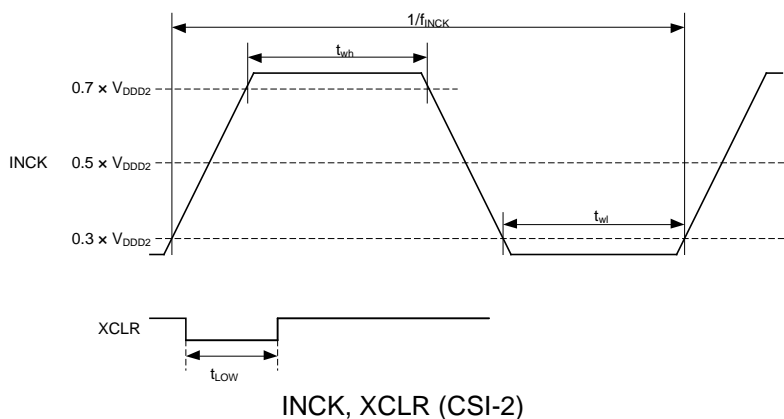
Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	187	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	396	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	1	mA	
Current consumption (Digital 3)	I_{DDD3}	—	—	36	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	190	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	25	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	20	μA	In the dark
Standby current (Digital 3)	$I_{DDD3STB}$	—	—	4	mA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage (CSI-2)

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DDSUB} , V_{DDHCM} , V_{DDHPX} , V_{DDHDA} , V_{DDHCP}	V_{ADD}	2.80	2.90	3.00	V
	Digital 1	$V_{DDL CN}$, $V_{DDL CM}$, $V_{DDL SA}$, $V_{DDL SC}$, $V_{DDL PL}$	V_{DDD1}	1.10	1.20	1.30	V
	Digital 2	V_{DDMIO} , V_{DDMPX}	V_{DDD2}	1.70	1.80	1.90	V
	Digital 3	$V_{DDL PLA}$, $V_{DDL PLD}$, $V_{DDL IF}$	V_{DDD3}	1.10	1.20	1.30	V
Digital input voltage	SDA, SCL		V_{IH1}	$0.7 \times V_{DDD2}$	—	$V_{DDD2} + 0.1$	V
			V_{IL1}	−0.1	—	$0.3 \times V_{DDD2}$	V
	XCLR, INCK SLASEL		V_{IH2}	$0.7 \times V_{DDD2}$	—	$V_{DDD2} + 0.1$	V
			V_{IL2}	−0.1	—	$0.3 \times V_{DDD2}$	V
Digital output voltage	XHS, XVS,		V_{HVOUT}	—	V_{DDD2}	—	V

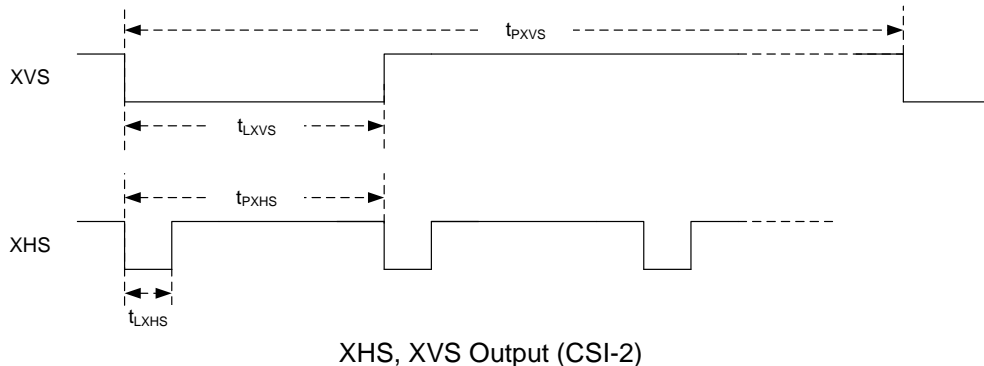
2. AC Characteristics (CSI-2)

INCK, XCLR (CSI-2)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	6	—	27	MHz	
INCK Low level pulse width	t_{wl}	5	—	—	ns	
INCK High level pulse width	t_{wh}	5	—	—	ns	
Clock duty	—	40	50	60	%	Criteria is $0.5 \times V_{\text{DD2}}$
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

XHS, XVS (Output) (CSI-2)

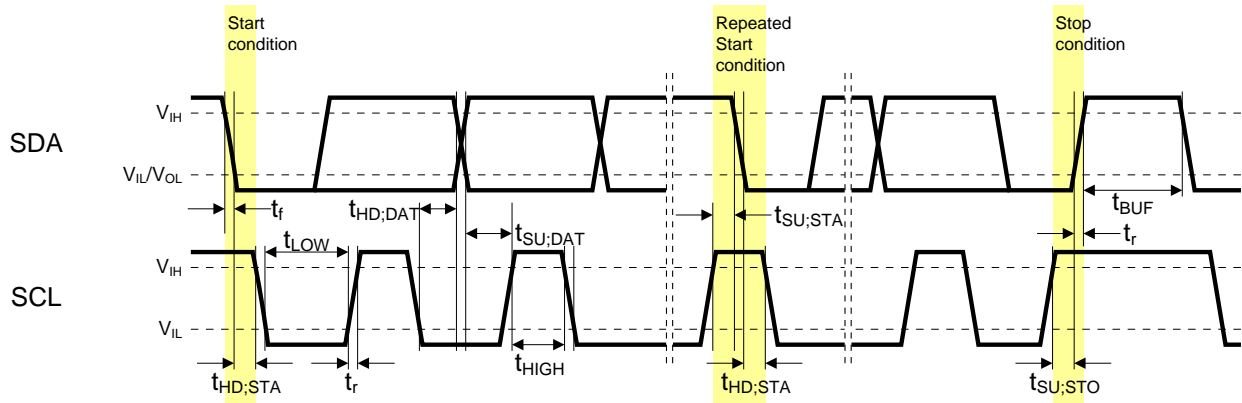


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{LXHS}		222		ns	16 clk @ 72MHz
XHS pulse period	t_{PXHS}		HMAX^{*1}		clk @ 72MHz	
XVS Low level pulse width	t_{LXVS}		t_{PXHS}		clk @ 72MHz	
XVS pulse period	t_{PXVS}		$\text{HMAX}^{*1} \times \text{VMAX}^{*2}$		clk @ 72MHz	

^{*1} The value set as HMAX (address 30ACh, bit [7:0] and address 30ADh, bit [7:0])

^{*2} The value set as VMAX (address 30A9h, bit [7:0], address 30AAh, bit [7:0] and address 30ABh, bit [3:0]).

I²C Communication (CSI-2)



I²C Communication (CSI-2)

I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.1	—	$0.3 \times V_{DD2}$	V	
High level input voltage	V_{IH}	$0.7 \times V_{DD2}$	—	$V_{DD2} + 0.1$	V	
Low level output voltage	V_{OL}	0	—	$0.2 \times V_{DD2}$	V	$V_{DD2} < 2$ V, Sink 3 mA
Output fall time	t_{of}	—	—	250	ns	Load 10 pF to 400 pF, $0.7 \times V_{DD2}$ to $0.3 \times V_{DD2}$
Input current (SCL, SDA, XCLR, INCK)	i_i	-10	—	10	μ A	$0.1 \times V_{DD2}$ to $0.9 \times V_{DD2}$
Input capacitance of SCL / SDA	C_i	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μ s
Low period of the SCL clock	t_{LOW}	1.3	—	—	μ s
High period of the SCL clock	t_{HIGH}	0.6	—	—	μ s
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μ s
Data hold time	$t_{HD;DAT}$	0	—	0.9	μ s
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μ s
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μ s

DCKP / DCKM, DMO (CSI-2)

Detailed explanation of CSI-2 interface is in following two documents, "MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.2" and "MIPI Alliance Specification for D-PHY Version 1.2".

Four data output Lanes are applied from MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) Version 1.2.

Electrical Characteristics When Using SLVS-EC

1. DC Characteristics (SLVS-EC)

Current Consumption and Gain Variable Range (SLVS-EC)

($V_{ADD} = 3.0\text{ V}$, $V_{DDD1} = 1.3\text{ V}$, $V_{DDD2} = 1.9\text{ V}$, $V_{DDD3} = 1.3\text{ V}$, $T_j = 60\text{ }^{\circ}\text{C}$, Reference Gain (0 dB)
Aspect ratio 4:3, mode0(All pixel scan mode, AD 14bit), 24 frame/s)

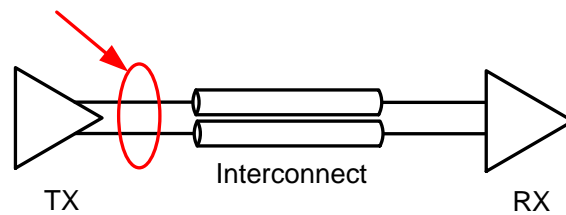
Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	187	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	490	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	1	mA	
Current consumption (Digital 3)	I_{DDD3}	—	—	69	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	190	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	25	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	20	μA	In the dark
Standby current (Digital 3)	$I_{DDD3STB}$	—	—	4	mA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage (SLVS-EC)

Item		Pins	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	Analog	V _{DD} SUB, V _{DD} HCM, V _{DD} HPX, V _{DD} HDA, V _{DD} HCP	V _{ADD}	2.80	2.90	3.00	V	
	Digital 1	V _{DD} LCN, V _{DD} LCM, V _{DD} LSA, V _{DD} LSC, V _{DD} LPL	V _{DDD1}	1.10	1.20	1.30	V	
	Digital 2	V _{DD} MIO, V _{DD} MPX	V _{DDD2}	1.70	1.80	1.90	V	
	Digital 3	V _{DD} LPLA, V _{DD} LPLD, V _{DD} LIF	V _{DDD3}	1.10	1.20	1.30	V	
Digital input voltage		XCLR, INCK, SCK, SDI, XCE, XHS, XVS	V _{IH}	0.7 × V _{DDD2}	—	V _{DDD2} + 0.1	V	
			V _{IL}	−0.1	—	0.3 × V _{DDD2}	V	
Digital input leakage current				I _{LI}	−1.0	—	1.0	μA

SLVS-EC Output DC Characteristics (SLVS-EC)

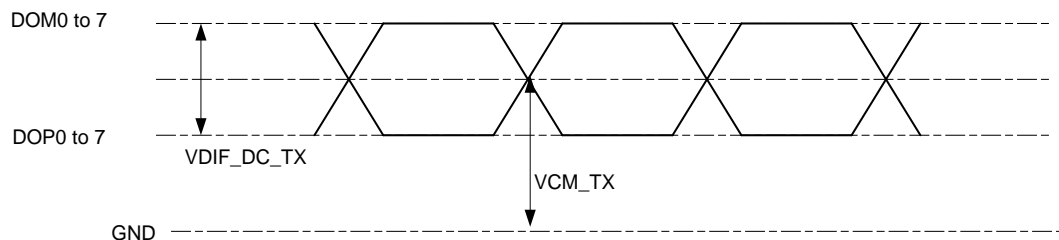
The characteristics of the TX of SLVS-EC are defined in the characteristic at the output pin of the package as shown in the figure below.



Definition of the characteristics of SLVS-EC (SLVS-EC)

The details about the SLVS-EC, please refer to the "SLVS-EC Specification".

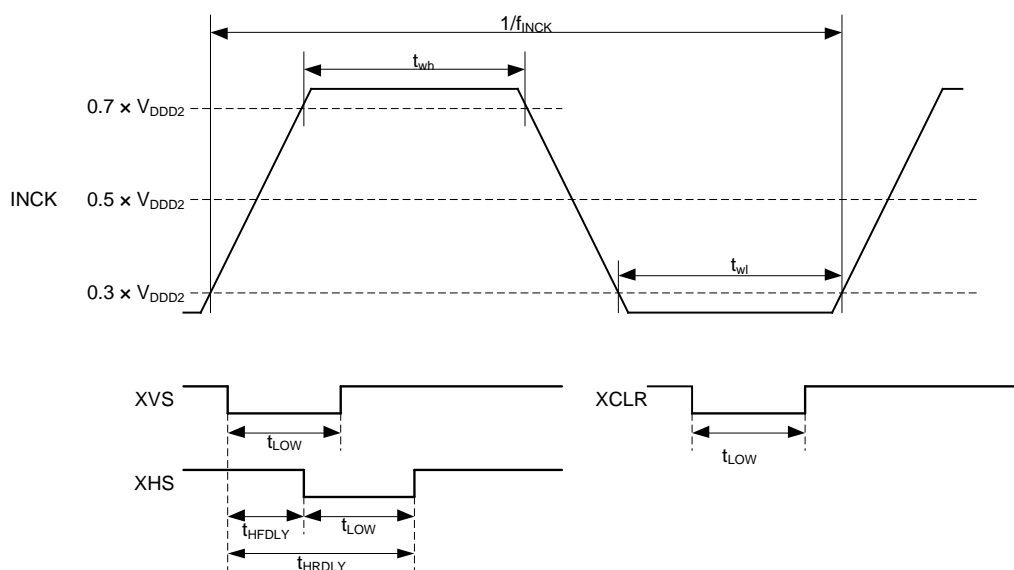
Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit
Digital output voltage	DOP0 to 7, DOM0 to 7	Differential DC Voltage	VDIF_DC_TX	160	—	280	mV
		Common Mode Voltage	VCM_TX	160	—	260	mV
		Single-ended Output Resistance	RSED_TX	30	—	60	Ω



DC output for TX of SLVS-EC (SLVS-EC)

2. AC Characteristics (SLVS-EC)

INCK, XCLR, XVS (input), XHS (input) (SLVS-EC)

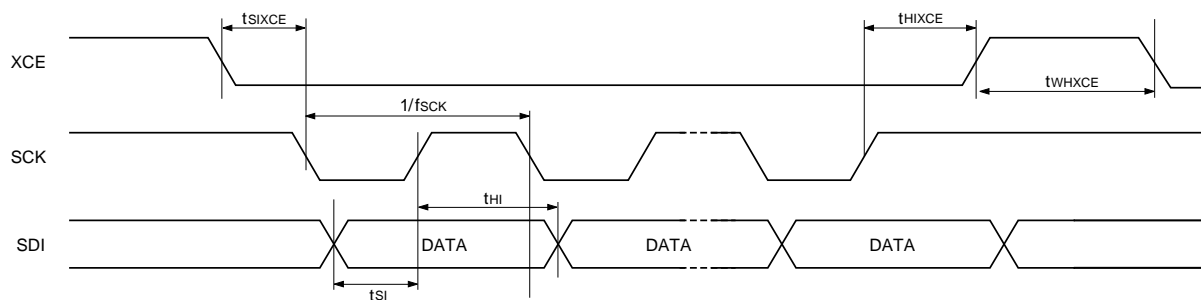


INCK, XCLR, XVS (input), XHS (input) (SLVS-EC)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	—	72.0	—	MHz	
INCK Low level pulse width	t_{wl}	5	—	—	ns	
INCK High level pulse width	t_{wh}	5	—	—	ns	
Clock duty	—	40	50	60	%	Criteria is $0.5 \times V_{\text{DD2}}$
Phase noise (100 kHz)	PN100K	—	—	-135	dBc/Hz	
Phase noise (1 MHz)	PN1M	—	—	-140	dBc/Hz	
Clock frequency error	FERR	-300	—	300	ppm	
XVS Low level pulse width	t_{LOW}	$4/f_{\text{INCK}}$	—	$12/f_{\text{INCK}}$	μs	
XHS Low level pulse width	t_{LOW}	$4/f_{\text{INCK}}$	—	$12/f_{\text{INCK}}$	μs	
XVS fall – XHS fall width	t_{HFDLY}	0	—	—	μs	
XVS fall – XHS rise width	t_{HRDLY}	$4/f_{\text{INCK}}$	—	$12/f_{\text{INCK}}$	μs	
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

Serial Communication

Serial Control Interface Timing

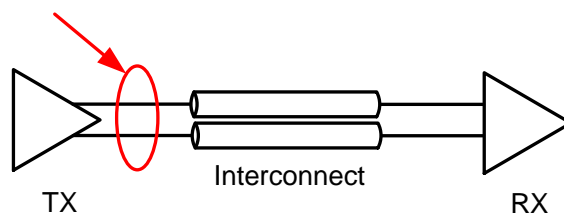


Serial Communication Characteristics (SLVS-EC)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	—	36	MHz
SDI input setup time	t_{SI}	7	—	—	ns
SDI input hold time	t_{HI}	7	—	—	ns
XCE input setup time	t_{SIXCE}	10	—	—	ns
XCE input hold time	t_{HIXCE}	10	—	—	ns
XCE High level pulse width	t_{WHXCE}	27	—	—	ns

SLVS-EC Output (SLVS-EC)

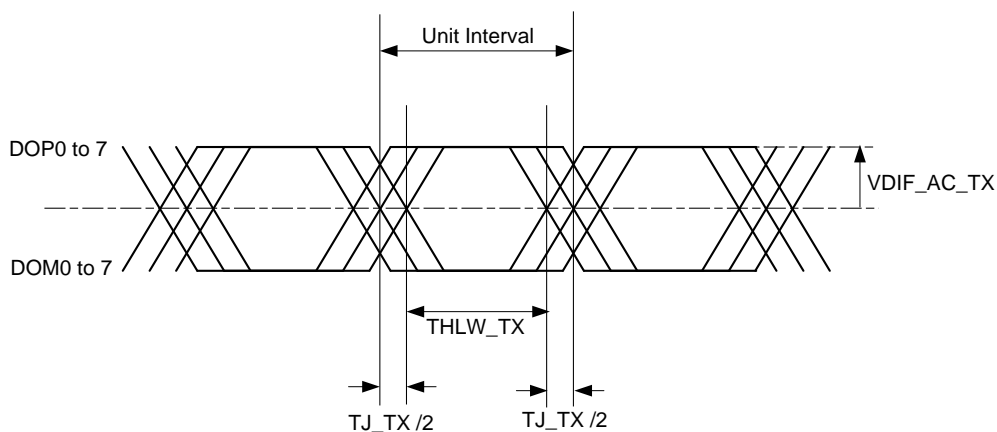
The characteristics of the TX of SLVS-EC are defined in the characteristic at the output pin of the package as shown in the figure below



Definition of the characteristics of SLVS-EC (SLVS-EC)

The details about the SLVS-EC, please refer to the "SLVS-EC Specification".

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Differential AC Voltage	VDIF_AC_TX	140	—	290	mV	100 Ω differential connection
Eye High / Low width	THLW_TX	0.2	—	—	UI	100 Ω differential connection
Deterministic Jitter	DJ_TX	—	—	0.3	UI	100 Ω differential connection
Total Jitter	TJ_TX	—	—	0.4	UI	100 Ω differential connection (BER $\leq 10^{-10}$)
Skew between the lanes	TLSKEW_TX	—	—	5	SI	



AC output for TX of SLVS-EC (SLVS-EC)

Spectral Sensitivity Characteristics (CSI-2 and SLVS-EC)

(Excludes lens characteristics and light source characteristics)

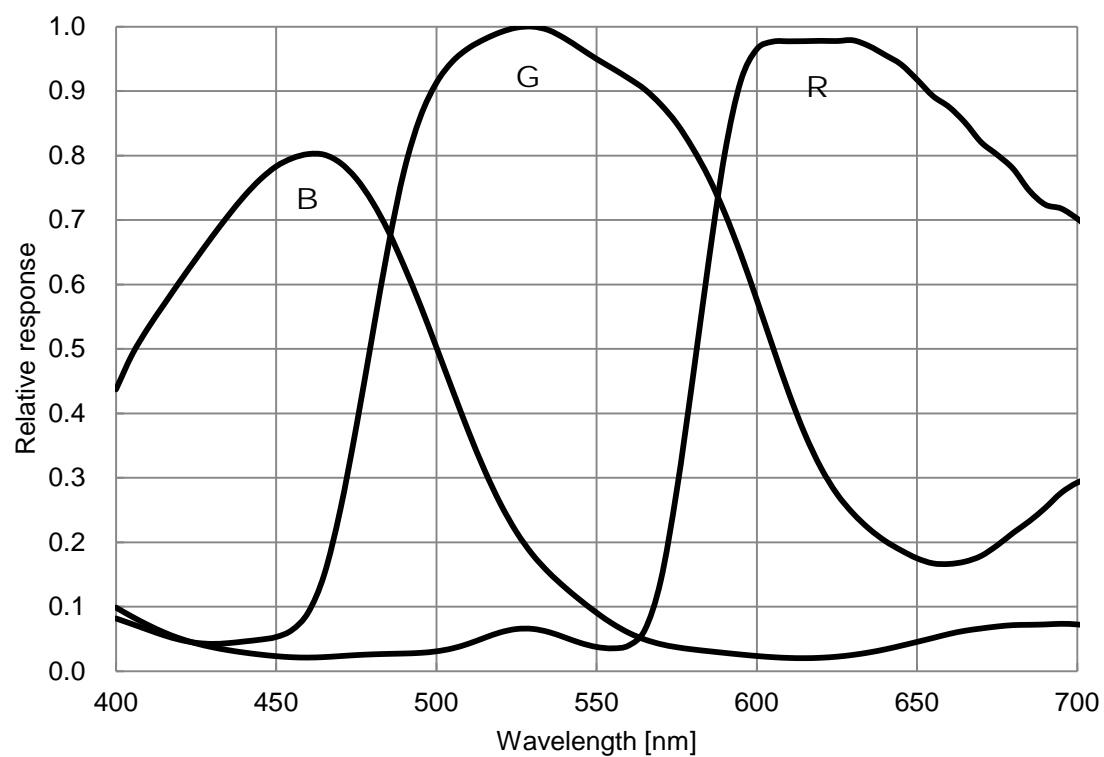


Image Sensor Characteristics (CSI-2 and SLVS-EC)

($V_{ADD} = 2.9\text{ V}$, $V_{DD1} = 1.2\text{ V}$, $V_{DD2} = 1.8\text{ V}$, $V_{DD3} = 1.2\text{ V}$, $T_j = 60\text{ }^{\circ}\text{C}$, 15 frame/s, Reference Gain (0 dB)
MCOVGAIN = 0h (Conversion gain Low))

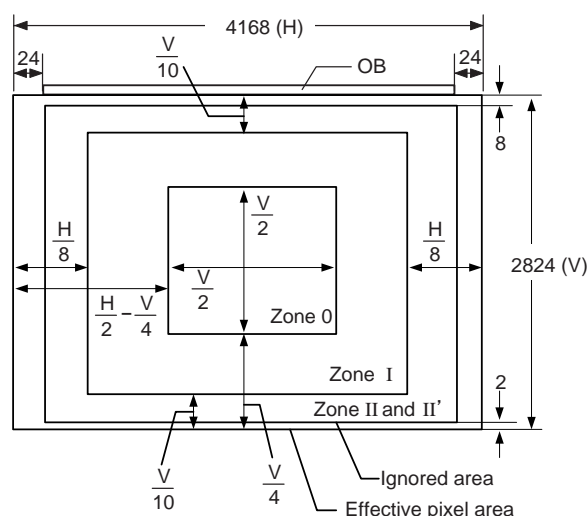
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity	Sg	1414	1768	2121	digit ^{*1}	1	1/30 s integration conversion value Zone 0
Sensitivity ratio	R	Rr	—	62	%	1	Zone 0
	B	Rb	—	48	%		
Saturation signal	Vsat	4095	—	—	digit ^{*1}	2	Zone 0 to II'
Video signal shading	SHg	—	—	20	%	3	Zone 0 and zone I
		—	—	25			Zone 0 to II'
Dark signal	Vdt	0	—	0.52	digit ^{*1}	4	1/30 s integration conversion value Zone 0 to II'
Dark signal shading	ΔVdt	0	—	0.71	digit ^{*1}	5	1/30 s integration conversion value Zone 0 to II'
Dark signal difference	VdOB	-0.25	—	0.25	digit ^{*1}	6	1/30 s integration conversion value Zone 0 to II'
Line crawl R	Lcr	-3.8	—	3.8	%	7	Zone 0 to II'
Line crawl B	Lcb	-3.8	—	3.8	%		
Conversion Gain high/low ratio	MCOVG	4.39	4.54	4.69	—	—	

^{*1} Shows digit when 12-bit output.

Example of digit conversion: 1 digit $\approx 0.237\text{ mV}$ when 12-bit output, 1 digit $\approx 0.948\text{ mV}$ when 10-bit output.

1. Zone Definition of Image Sensor Characteristics

Zone definition of image sensor characteristics and reference position during dark signal measurement are shown below.



Zone Definition of Image Sensor Characteristics and Reference Position during Dark Signal Measurement

Image Sensor Characteristics Measurement Method (CSI-2 and SLVS-EC)

1. Measurement Conditions

- (1) In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
- (2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

2. Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. When readout the image, four adjacent pixels with same color are added and regarded as one pixel, and the Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram and Readout Image

3. Definition of Standard Imaging Conditions

- ◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m², color temperature of 3200 K halogen source) as a subject.
(Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.
- ◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles.
Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.
- ◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles.
Use a testing standard lens (exit pupil distance -54 mm) with CM500S (t = 1.0 mm) as an IR cut filter.
The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, Sensitivity ratio

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/640 s, measure the Gr, Gb, R and B signal outputs (VGr, VGb, VR and VB) at the center of the screen which is zone 0, and substitute the values into the following formula

$$VG = (VGr + VGb) / 2$$

$$Sg = VG \times 640/30 \text{ [digit]}$$

$$Rr = VR/VG \times 100 \text{ [%]}$$

$$Rb = VB/VG \times 100 \text{ [%]}$$

2. Saturation signal

Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times the intensity with the average value of the G (= (Gr + Gb)/2) signal output, 1768 digit when 12-bit output (442 digit when 10-bit output). Measure the minimum values of the Gr, Gb, R and B signals when shooting in rolling shutter mode.

3. Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the G signal output is 1768 digit when 12-bit output (442 digit when 10-bit output). Then measure the maximum value (Gmax [digit]) and the minimum value (Gmin [digit]) of the G signal output, and substitute the values into the following formula.

- When 10-bit output

$$SHg = (G_{max} - G_{min}) / 442 \times 100 [\%]$$
- When 12-bit output

$$SHg = (G_{max} - G_{min}) / 1768 \times 100 [\%]$$

4. Dark signal

Measure the average value (Vdt [digit]) of the signal output in zone 0 to zone II' in the light-obstructed state. Define the average value of the signal output accumulated in 1 frame period (t1v) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: t1h) as Vdt1H, and then substitute the values into the following formula.

$$Vdt = (Vdt1V - Vdt1H) / (t1v - t1h) / 30 [\text{digit}]$$

5. Dark signal shading

Following the item 4, measure the maximum value (Vdmax [digit]) and minimum value (Vdmin [digit]) of the dark signal output, and substitute the values into the following formula.

$$\Delta Vdt = Vd_{max} - Vd_{min} [\text{digit}]$$

6. Dark signal difference

Following the item 5, measure the average value of the dark signal output (VdOB [digit]) in zone 0 to zone II' using the optical black level as a reference.

7. Line crawl

Set the measurement condition to the standard imaging condition III. After adjusting the average value of the G (= (Gr + Gb) / 2) signal output when inserting G filter to 1768 digit when 12-bit output (442 digit when 10-bit output), measure the average values of the Gr and Gb signal output (GGr, GGb).

After adjusting the average value of the R signal output when inserting R filter to 1768 digit when 12-bit output (442 digit when 10-bit output), measure the average values of the Gr and Gb signal output (RGr, RGb). Substitute the values into the following formula.

$$Lcr = \{RGr - (GGr / GGb) \times RGb\} / \{[RGr + (GGr / GGb) \times RGb] / 2\} \times 100 [\%]$$

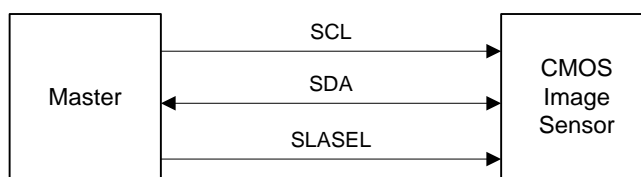
Then, after adjusting the average value of the B signal output when inserting B filter to 1768 digit when 12-bit output (442 digit when 10-bit output), measure the average values of the Gr and Gb signal output (BGr, BGb). Substitute the values into the following formula.

$$Lcb = \{BGb - (GGb / GGr) \times BGr\} / \{[BGb + (GGb / GGr) \times BGr] / 2\} \times 100 [\%]$$

Setting Registers Using I²C Communication (When Using CSI-2)

Description of Setting Registers When Using I²C Communication

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The slave address is selectable by pin connection of SLASEL.

SLAVE Address

SLASEL (Pin No. W5)	Slave address							
	MSB							LSB
Low	0	0	1	0	0	0	0	R / W ^{*1}
High or NC	0	0	1	1	0	1	0	R / W ^{*1}

^{*1} R/W is data direction bit

R / W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

Pin Connection of Serial Communication Operation Specifications When Using I²C Communication

The pin connection of serial communication method conforms to the Camera Control Instance (CCI). CCI is an I²C fast-mode compatible interface, and the data transfer protocol is I²C standard.

This pin connection of serial communication circuit can be used to access the control-registers and status-registers of the sensor.

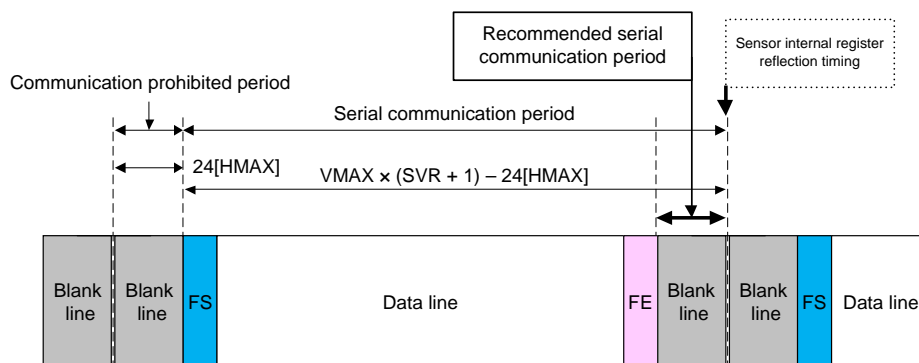
I²C pin description

Symbol	Pin No.	Remarks
SCL	P20	Serial clock input
SDA	R20	Serial data communication

Register Communication Timing When Using I²C Communication

In I²C communication system, register setting can be performed during the period when communication is from the following figure “ $V_{MAX} \times (SVR + 1) - 24 [H_{MAX}]$ ”.

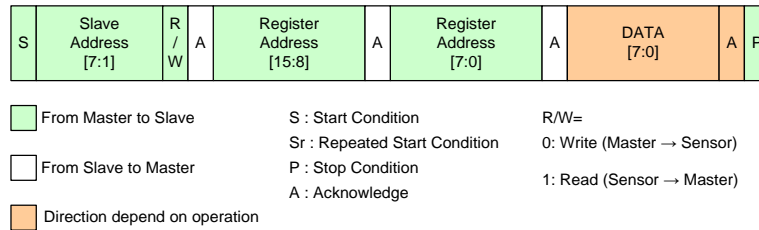
Perform I²C communication within “FS of next frame – 24 [HMAX]” period (recommended serial communication period) after FE period end to prevent noise. However, for non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), then register communication can be performed other than during the recommended serial communication period of those frames.



Register Communication Timing When Using I²C Communication

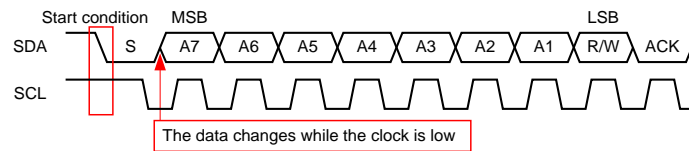
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

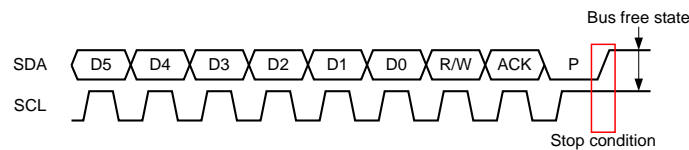


I²C Communication Protocol

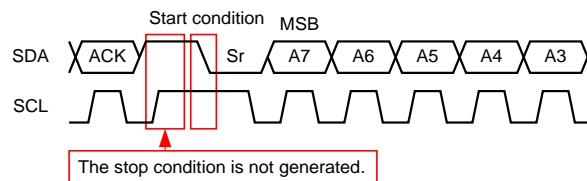
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) is transferred. Data is transferred at the clock cycle of SCL. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

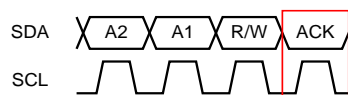


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge and release (does not drive) SDA.



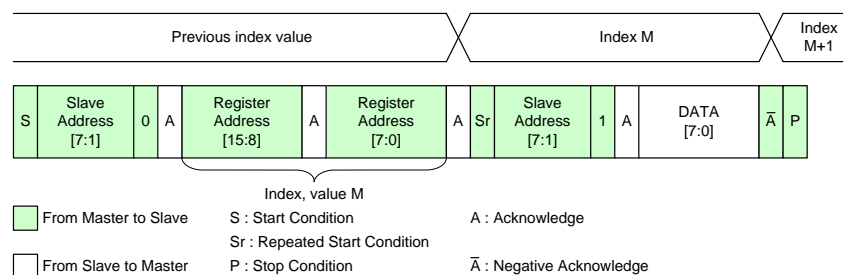
Acknowledge

Register Write and Read

This sensor supports to four read operations and two write operations.
In addition, INCK signal must be driven during the I²C serial communication period.

Single Read from Random Location

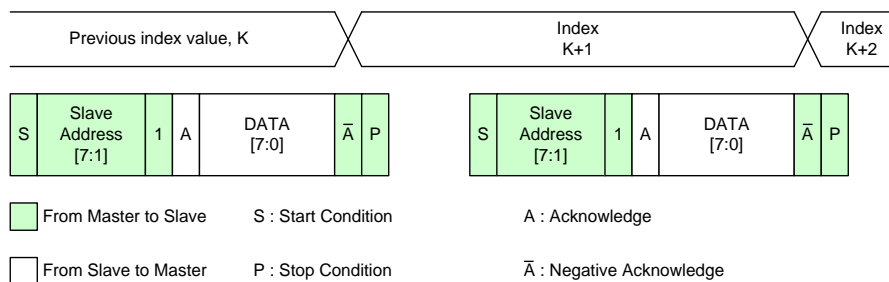
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

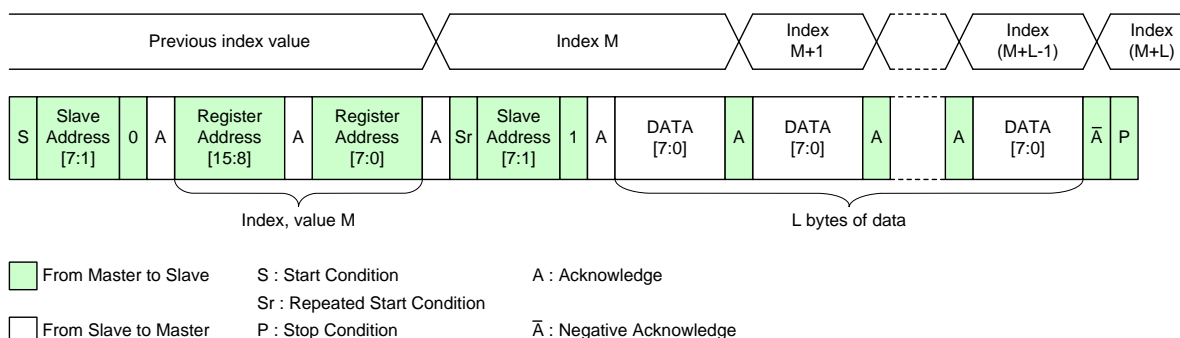
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

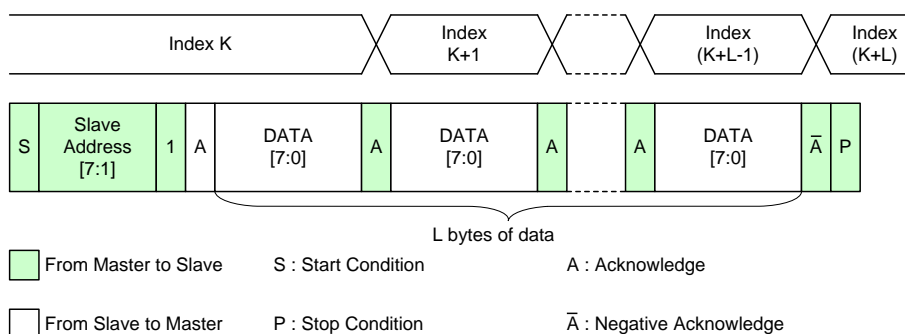
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

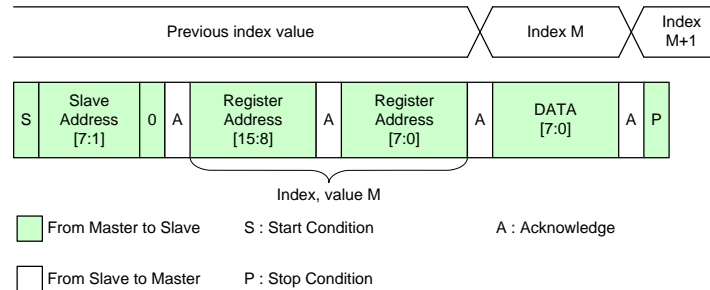
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

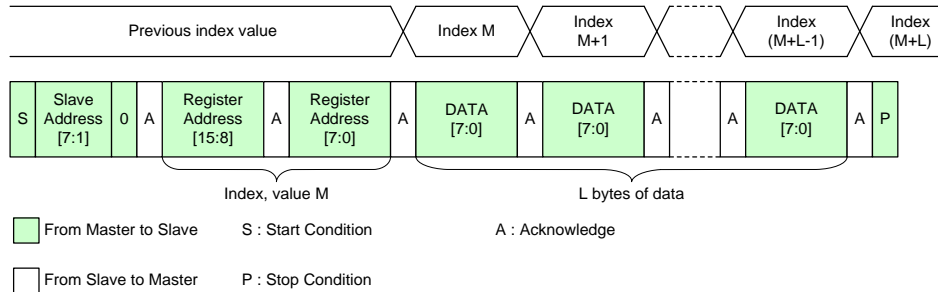
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



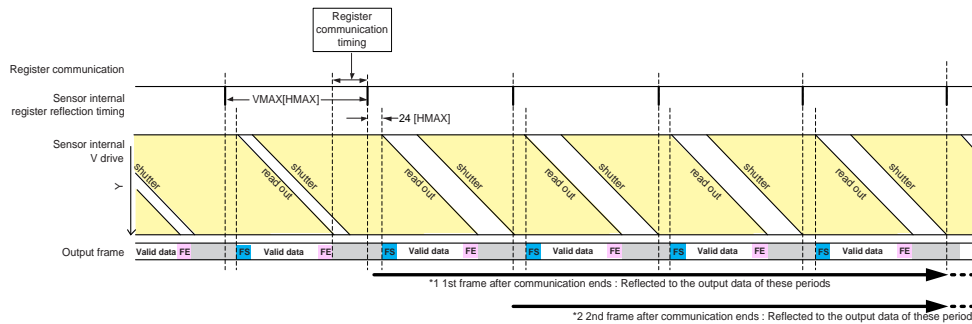
Sequential Write Starting from Random Location

Register Value Reflection Timing to Output Data

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1 1st frame after communication ends	The communication contents are reflected to the output data from 1st frame after communication ends.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from 2nd frame after communication ends.
Immediately	The communication contents are reflected immediately.

For which reflection timing of each register, see “Register Map” on pages 43 to 48.



Register Value Reflection Timing to Output Data

Register Hold Setting

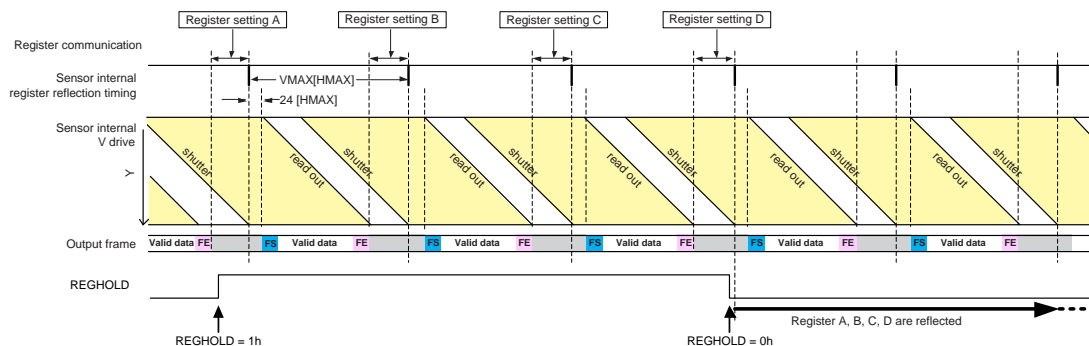
Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD for the registers of which reflection timing is frame unit (*1 and *2).

Registers are set when REGHOLD = 1h, and REGHOLD is set to “0h” during communication period just before the frame the registers are reflected from.

Register hold function is invalid for the registers of which reflection timing is immediately. Therefore these registers are reflected immediately when even though REGHOLD = 1h.

REGHOLD Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
REGHOLD	302Bh	—	[0]	0h	Normal communication Reflecting register setting when register settings are held
				1h	Register setting hold



Example of REGHOLD operation

Setting Registers Using Serial Communication (When Using SLVS-EC)

Setting Registers Using Serial Communication (SLVS-EC)

Sensor operation is controlled by the register settings. Follow the procedure below and make the register settings by serial communication.

1. Set XCE Low to enable the chip's serial communication function.
2. Transmit serial data (SDI) synchronized with SCK 1 bit at a time from the lower bits.
3. Transmit the Chip ID (fixed value: 81h) in the first byte.
4. Transmit the address value of the register to be set in the second and third bytes.
5. Transmit the register setting value to the address designated by the second and third bytes in the fourth byte.
6. Transmit the register setting value to the address following the address designated by the second and third bytes in the fifth byte.
7. Transmit the register setting values to subsequent addresses in order thereafter.
8. Set XCE High to end serial communication.

The sensor clears the Chip ID and address setting data by setting XCE High.

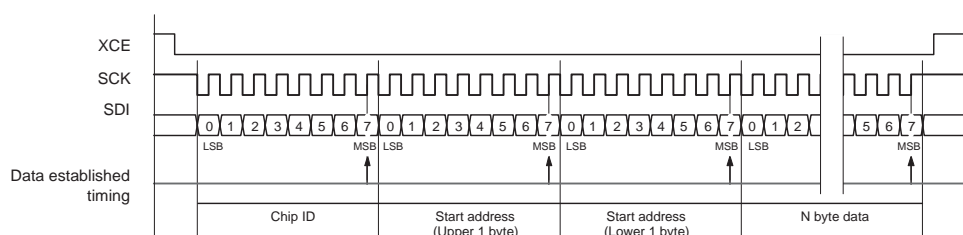
Therefore, the Chip ID and address settings must also be made when the next serial communication is performed. Continuous write across upper bytes is prohibited. When writing across upper bytes, first complete the above sequence, and then perform communication again. In addition, when jumping to a discontinuous address, also first complete the above sequence, and then perform communication again.

Perform serial communication within the 3XHS period (recommended serial communication period) after the fall of XVS to avoid affecting the image quality.

Settings made by serial communication are basically updated immediately each time 1 byte of setting values is transmitted. However, in some exceptional cases (electronic shutter setting, etc.), register setting values are updated immediately before the start of readout immediately after the recommended serial communication period (4th XHS). For details, see "Register Map" on pages 43 to 48 and "Register Value Reflection Timing to Output Data" on page 42.

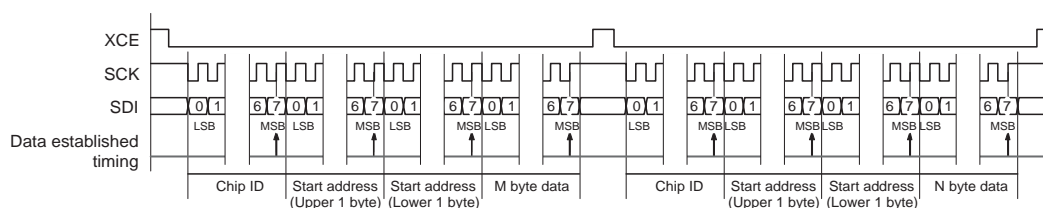
- Note) 1. Communication is always accepted.
2. Communication should be completed within the recommended serial communication period to prevent noise. However, this restriction does not apply during the readout period of non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), so register communication can be performed other than during the communication period of those frames.

Example of Serial Communication Timing 1



Example of Serial Communication 1

Example of Serial Communication Timing 2



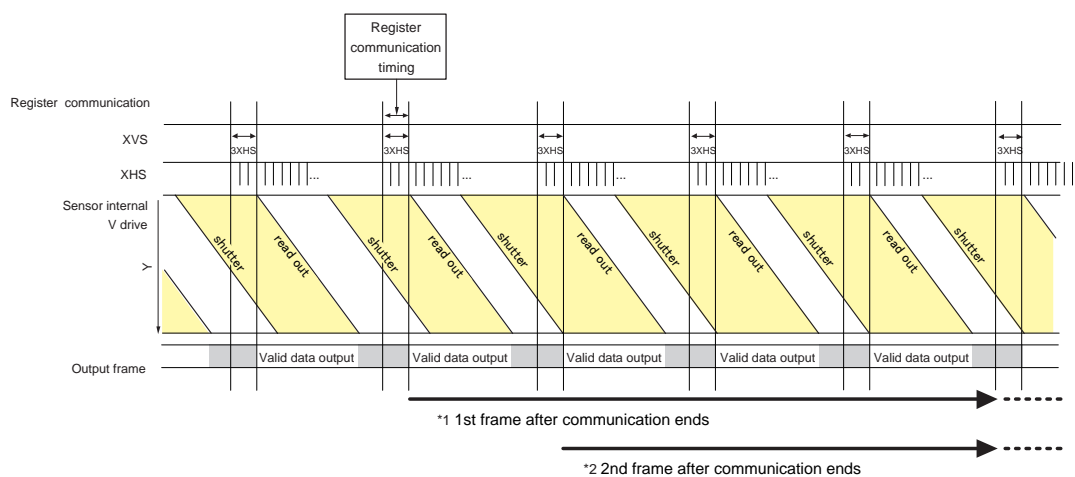
Example of Serial Communication 2

Register Value Reflection Timing to Output Data (SLVS-EC)

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Description
*1 1st frame after communication ends	The communication contents are reflected to the output data from the V period during which communication was performed.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from the next V period after the V period during which communication was performed.

For which reflection timing of each register, see “Register Map” on pages 43 to 48.



Register Value Reflection Timing to Output Data (SLVS-EC)

Register Map

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-EC						
3000h	0000h	[0]	1h	Immediately	STANDBY	0h : Normal operation 1h : Overall standby	Setting range: 0h to 1h
		[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communication block	Setting range: 0h to 1h
		[2]	0h			—	Set the default value.
		[3]	0h	Immediately	STBMIPI	0h: CSI-2 on 1h: CSI-2 standby	CSI-2: set to 0h SLVS-EC: set to 1h
		[4]	1h	Immediately	STBDV	0h: Normal operation 1h: Frequency demultiplier standby	Setting range: 0h to 1h
		[7:5]	0h			—	Set the default value.
3001h	0001h	[0]	0h	Immediately	MDCHGRST	When changing from 0h to 1h: SLVS-EC I/F reset (Training Sequence starts)	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
		[3:1]	0h			—	Set the default value.
		[4]	0h	*1	CLPSQRST	When changing from 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
		[7:5]	0h			—	Set the default value.
—	0002h	[0]	0h	*1	SSBRK	SLVS-EC only When changing from 0h to 1h: Interrupt enable	Setting range: 0h to 1h After the interrupt, the value is automatically returned to 0h.
		[7:1]	00h			—	Set the default value.
—	0003h	[3:0]	0h			—	Set the default value.
		[6:4]	2h	*1	LANESEL	SLVS-EC only 0h: 8Lane, 1h: 6Lane, 2h: 4Lane, 3h: 2Lane, 4h: 1Lane, Others: Prohibited	Setting range: 0h to 4h
		[7]	0h			—	Set the default value.
3004h	0004h	[7:0]	10h	*1	MDSEL1	Mode select 1	Set the value according to each readout mode register setting.
3005h	0005h	[7:0]	35h	*1	MDSEL2	Mode select 2	Set the value according to each readout mode register setting.
3006h	0006h	[7:0]	02h	*1	MDSEL3	Mode select 3	Set the value according to each readout mode register setting.
3007h	0007h	[7:0]	A0h	*1	MDSEL4	Mode select 4	Set the value according to each readout mode register setting.
3008h	0008h	[0]	0h	*1	SMD	0h: Rolling shutter 1h: Global reset shutter	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
300Ah	000Ah	[7:0]	000h	*1	PGC	Analog gain setting	Setting range: 000h to 7A5h
300Bh	000Bh	[2:0]					
		[7:3]	00h			—	Set the default value.
300Eh	000Eh	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0000h to FFFFh
300Fh	000Fh	[7:0]					
3012h	0012h	[3:0]	0h	*1	DGAIN	Digital gain setting 0h: 0dB, 1h: +6dB, 2h: +12dB, 3h: +18dB, Others: Prohibited	Setting range: 0h to 3h
		[7:4]	0h			—	Set the default value.
3017h	—	[1:0]	3h	Immediately	SYNCDRV	CSI-2 only XHS/XVS pulse output enable 0h: XHS/XVS is output 3h: XHS/XVS is Hi-Z	Refer to the "Standby Cancel Sequence" when using XHS/XVS output
		[7:2]	2Ah			—	Set the default value.
3019h	0019h	[0]	0h	*2	MDVREV	0h : Vertical direction normal readout 1h : Vertical direction inversion readout	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-EC						
302Bh	—	[0]	0h	Immediately	REGHOLD	CSI-2 only Register setting hold function	Setting range is shown in "Description of Registers"
		[7:1]	00h			—	Set the default value.
302Ch	002Ch	[7:0]	0005h	*2	SHR	Specifies the integration start horizontal period	Setting range is shown in "Description of Registers"
302Dh	002Dh	[7:0]					
3030h	0030h	[7:0]	77h	*1	MDSEL5	Mode select 5	Set the value according to each readout mode register setting.
3033h	0033h	[3:0]	0h			—	Set the default value.
		[4]	1h	Immediately	XMSTA	CSI-2 only Master mode operation 0h: Master mode start 1h: Master mode stop	Refer to the "Standby Cancel Sequence"
		[5]	0h	Immediately	MSTSLV	Master / Slave Switching 0h: Slave mode 1h: Master mode	Refer to the "Standby Cancel Sequence"
		[7:6]	0h			—	Set the default value.
3034h	0034h	[0]	1h	*1	HOPBOUT_EN	HOPB output 0h:no output 1:output	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
3035h	0035h	[0]	0h	*1	HTRIMMING_EN	Horizontal arbitrary cropping enable	Setting range is shown in "Description of Registers"
		[7:1]	00h			—	Set the default value.
3036h	0036h	[7:0]	0000h	*1	HTRIMMING_START	Horizontal cropping start position	Setting range is shown in "Description of Registers"
3037h	0037h	[5:0]					
		[7:6]	0h			—	Set the default value.
3038h	0038h	[7:0]	0000h	*1	HTRIMMING_END	Horizontal cropping end position + 1	Setting range is shown in "Description of Registers"
3039h	0039h	[5:0]					
		[7:6]	0h			—	Set the default value.
303Ch	003Ch	[1:0]	2h	Immediately	SYS_MODE	Select use Interface 0h: SLVS-EC / 1h: MIPI1.728Gbps	Refer to the "Standby Cancel Sequence" Setting range: 0h to 1h
		[7:2]	00h			—	Set the default value.
3042h	0042h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 0h to FFh 10-bit readout mode: 1 digit/1h 12-bit readout mode: 4 digit/1h 14-bit readout mode: 16 digit/1h
3047h	0047h	[7:0]	00h	*1	PLSTMG11	Drive pulse timing setting 11	Set to 01h
304Eh	004Eh	[7:0]	1Eh	immediately	PLSTMG12	Drive pulse timing setting 12	Set to 0Bh
304Fh	004Fh	[7:0]	37h	immediately	PLSTMG13	Drive pulse timing setting 13	Set to 24h
3061h	0061h	[0]	0h	Immediately	LESS_SHUT	Shutter less mode switch 0h: Shutter less mode OFF 1h: Shutter less mode ON	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
3062h	0062h	[7:0]	06h	immediately	PLSTMG14	Drive pulse timing setting 14	Set to 25h
3064h	0064h	[7:0]	40h	immediately	PLSTMG15	Drive pulse timing setting 15	Set to 78h
3065h	0065h	[7:0]	0Ch	immediately	PLSTMG16	Drive pulse timing setting 16	Set to 33h
3067h	0067h	[7:0]	34h	immediately	PLSTMG17	Drive pulse timing setting 17	Set to 71h
3068h	0068h	[7:0]	001Ah	immediately	MDSEL15	Mode select 15	Set the value according to each readout mode register setting.
3069h	0069h	[7:0]					
—	006Eh	[7:0]	0AAh	*1	SYNC_SYMBOL	SLVS-EC only Sets the symbol following the comma symbol within the sync code	Setting range: 000h to 1FFh
—	006Fh	[0]					
		[7:1]	00h			—	Set the default value.
—	0070h	[7:0]	060h	*1	DESKEW_SYMBOL	SLVS-EC only Set the symbol following the comma symbol within deskew code	Setting range: 000h to 1FFh
—	0071h	[0]					
		[7:1]	00h			—	Set the default value.
—	0072h	[7:0]	000h	*1	IDLE_CODE1	SLVS-EC only Sets the Idle code 1 symbol	Setting range: 000h to 1FFh
—	0073h	[0]					
		[7:1]	00h			—	Set the default value.
—	0074h	[7:0]	000h	*1	IDLE_CODE2	SLVS-EC only Sets the Idle code 2 symbol	Setting range: 000h to 1FFh
—	0075h	[0]					
		[7:1]	00h			—	Set the default value.
—	0076h	[7:0]	000h	*1	IDLE_CODE3	SLVS-EC only Sets the Idle code 3 symbol	Setting range: 000h to 1FFh
—	0077h	[0]					
		[7:1]	00h			—	Set the default value.
—	0078h	[7:0]	000h	*1	IDLE_CODE4	SLVS-EC only Sets the Idle code 4 symbol	Setting range: 000h to 1FFh
—	0079h	[0]					
		[7:1]	00h			—	Set the default value.

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-E C						
3080h	0080h	[7:0]	00h	*1	MDSEL6	Mode select 6	Set the value according to each readout mode register setting.
3081h	0081h	[7:0]	01h	*1	MDSEL7	Mode select 7	Set the value according to each readout mode register setting.
3084h	0084h	[7:0]	01E6h	*1	HCOUNT1	Timing setting in 1XHS period 1	Set the value according to each readout mode register setting.
3085h	0085h	[7:0]					
3086h	0086h	[7:0]	01E6h	*1	HCOUNT2	Timing setting in 1XHS period 2	Set the value according to each readout mode register setting.
3087h	0087h	[7:0]					
3088h	0088h	[7:0]	0Ch	immediately	PLSTMG18	Drive pulse timing setting 18	Set to 75h
308Ah	008Ah	[7:0]	011Ch	immediately	PLSTMG19	Drive pulse timing setting 19	Set to 0109h
308Bh	008Bh	[7:0]					
308Ch	008Ch	[7:0]	16h	immediately	PLSTMG20	Drive pulse timing setting 20	Set to 61h
3092h	0092h	[0]	0h	*1	MCOVGAIN	Conversion gain switching register 0h: Conversion gain low 1h: Conversion gain High	Setting range: 0h to 1h
		[7:1]	00h				
30A8h	00A8h	[7:0]	02h	*1	MDSEL8	Mode select 8	Set the value according to each readout mode register setting.
30A9h	—	[7:0]	001F2h	*1	VMAX	CSI-2 only Vertical drive period length	Setting range is shown in "Description of Registers"
30AAh	—	[7:0]					
30ABh	—	[3:0]	00h			—	Set the default value.
		[7:4]					
30ACh	—	[7:0]	01E6h	*1	HMAX	CSI-2 only Horizontal drive period length	Setting range is shown in "Description of Registers"
30ADh	—	[7:0]					
30DDh	00DDh	[0]	0h	*1	VWIDCUTEN	Vertical arbitrary cropping enable	Setting range is shown in "Description of Registers"
		[7:1]	00h				
30DEh	00DEh	[7:0]	0000h	*1	VWIDCUT	Width of vertical arbitrary cropping	Setting range is shown in "Description of Registers"
30DFh	00DFh	[5:0]					
		[7:6]	0h			—	Set the default value.
30E0h	00E0h	[7:0]	0000h	*1	VWINPOS	Start position of vertical arbitrary cropping (two's complement)	Setting range is shown in "Description of Registers"
30E1h	00E1h	[5:0]					
30E2h	00E2h	[7:0]	00h	*1	VCUTMODE	Mode setting register	Set the value according to each readout mode register setting.
		[7:0]					
—	00EAh	[7:0]	003h	*1	STANDBY_SYMBOL	SLVS-EC only Sets the symbol following the comma symbol within the standby code	Setting range: 000h to 1FFh
—	00EBh	[0]					
—	00F4h	[7:1]	00h			—	Set the default value.
		[0]	0h	*1	CRCEN	SLVS-EC only CRC insertion at the end of line 0h: Without CRC insertion 1h: With CRC insertion	Setting range: 0h to 1h ECCEN and CRCEN cannot be used together.
—	00F5h	[7:1]	00h			—	Set the default value.
		[0]	0h	*1	ECCEN	SLVS-EC only ECC insertion in lines 0h: Without ECC (ECC Option = 0) 1h: With ECC (ECC Option =1) 2h: With ECC (ECC Option =2) 3h: Prohibited	Setting range: 0h to 2h ECCEN and CRCEN cannot be used together.
310Bh	010Bh	[1:0]	2h	*1		—	Set the default value.
		[7:2]	00h			—	Set the default value.
		[0]	0h	immediately	STBPL_IF	PLL standby control register for IF	Refer to the "Standby Cancel Sequence"
		[3:1]	0h			—	Set the default value.
—	0114h	[4]	0h	immediately	STBPL_AD	PLL standby control register for AD	Refer to the "Standby Cancel Sequence"
		[7:5]	0h			—	Set the default value.
—	0115h	[4:0]	0Ah	*1	INIT_LENGTH	SLVS-EC only Sets the length of low output period during mode change and initialization	Setting range: 01h to 10h UNIT: SI
—	0116h	[7:5]	0h			—	Set the default value.
—	0117h	[7:0]	007FFh	*1	SYNC_LENGTH	SLVS-EC only Sets sync code repeat count in training sequence	Setting range: 000001h to 007FFFh UNIT: 4xSI
—	0118h	[7:0]					
—	0119h	[7:0]	10h	*1	DESKEW_INTERVAL	SLVS-EC only Sets idle code repeat count between deskew codes in training sequence	Setting range: 03h to FFh UNIT: SI
—	0119h	[7:0]	10h	*1	STANDBY_LENGTH	SLVS-EC only Sets standby code repeat count in standby sequence	Setting range: 03h to FFh UNIT: 4xSI

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-E C						
—	011Ah	[7:0]	10h	*1	DESKEW_LENGTH	SLVS-EC only Sets deskew code repeat count in training sequence	Setting range: 01h to FFh
311Fh	011Fh	[7:0]	00h	immediately	PLRD10	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3122h	0122h	[7:0]	01h	immediately	PLRD2	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3123h	0123h	[7:0]	00h	immediately	PLRD11	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3124h	0124h	[7:0]	00h	immediately	PLRD12	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3125h	0125h	[7:0]	01h	immediately	PLRD13	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3127h	0127h	[7:0]	02h	immediately	PLRD14	Input clock frequency setting register	Setting range is shown in "Description of Registers"
3129h	0129h	[7:0]	60h	immediately	PLRD3	Input clock frequency setting register	Setting range is shown in "Description of Registers"
312Ah	012Ah	[7:0]	01h	immediately	PLRD4	Input clock frequency setting register	Setting range is shown in "Description of Registers"
312Dh	012Dh	[7:0]	02h	immediately	PLRD15	Input clock frequency setting register	Setting range is shown in "Description of Registers"
312Fh	—	[5:0]	04h	*1	OPB_SIZE_V	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
		[7:6]	0h			—	Set the default value.
3130h	—	[7:0]	03B4h	*1	WRITE_VSIZE	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
3131h	—	[4:0]				—	Set the default value.
3132h	—	[7:0]	03B0h	*1	Y_OUT_SIZE	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
3133h	—	[4:0]				—	Set the default value.
3134h	0134h	[7:0]	00A7h	*1	tclkpost	Global timing register	Set to 00AFh
3135h	0135h	[7:0]					
3136h	0136h	[7:0]	009Fh	*1	thszero	Global timing register	Set to 00C7h
3137h	0137h	[7:0]					
3138h	0138h	[7:0]	006Fh	*1	thsprepare	Global timing register	Set to 007Fh
3139h	0139h	[7:0]					
313Ah	013Ah	[7:0]	005Fh	*1	tclktrail	Global timing register	Set to 006Fh
313Bh	013Bh	[7:0]					
313Ch	013Ch	[7:0]	005Fh	*1	thstrail	Global timing register	Set to 006Fh
313Dh	013Dh	[7:0]					
313Eh	013Eh	[7:0]	017Fh	*1	tclkzero	Global timing register	Set to 01CFh
313Fh	013Fh	[7:0]					
3140h	0140h	[7:0]	006Fh	*1	tclkprepare	Global timing register	Set to 0077h
3141h	0141h	[7:0]					
3142h	0142h	[7:0]	004Fh	*1	tlpx	Global timing register	Set to 005Fh
3143h	0143h	[7:0]					
3146h	0146h	[7:0]	01h	immediately	PLSTMG10	Drive pulse timing setting 10	Set to 00h
31E8h	01E8h	[7:0]	00A0h	immediately	PLRD1	Input clock frequency setting register	Setting range is shown in "Description of Registers"
31E9h	01E9h	[7:0]					
3234h	0234h	[7:0]	0021h	immediately	PLSTMG21	Drive pulse timing setting 21	Set to 0032h
3235h	0235h	[7:0]					
3248h	0248h	[7:0]	00C0h	immediately	PLSTMG22	Drive pulse timing setting 22	Set to 00BCh
3249h	0249h	[7:0]					
3250h	0250h	[7:0]	00C0h	immediately	PLSTMG23	Drive pulse timing setting 23	Set to 00BCh
3251h	0251h	[7:0]					
3258h	0258h	[7:0]	00C0h	immediately	PLSTMG24	Drive pulse timing setting 24	Set to 00BCh
3259h	0259h	[7:0]					
3260h	0260h	[7:0]	00C0h	immediately	PLSTMG25	Drive pulse timing setting 25	Set to 00BCh
3261h	0261h	[7:0]					
3274h	0274h	[7:0]	0017h	immediately	PLSTMG26	Drive pulse timing setting 26	Set to 0013h
3275h	0275h	[7:0]					
3276h	0276h	[7:0]	0000h	immediately	PLSTMG27	Drive pulse timing setting 27	Set to 001Fh
3277h	0277h	[7:0]					
3278h	0278h	[7:0]	0000h	immediately	PLSTMG28	Drive pulse timing setting 28	Set to 0030h
3279h	0279h	[7:0]					
327Ch	027Ch	[7:0]	0017h	immediately	PLSTMG29	Drive pulse timing setting 29	Set to 0013h
327Dh	027Dh	[7:0]					
327Eh	027Eh	[7:0]	0000h	immediately	PLSTMG30	Drive pulse timing setting 30	Set to 001Fh
327Fh	027Fh	[7:0]					
3280h	0280h	[7:0]	0000h	immediately	PLSTMG31	Drive pulse timing setting 31	Set to 0030h
3281h	0281h	[7:0]					

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-E C						
3284h	0284h	[7:0]	0017h	immediately	PLSTMG32	Drive pulse timing setting 32	Set to 0013h
3285h	0285h	[7:0]					
3286h	0286h	[7:0]					
3287h	0287h	[7:0]	0000h	immediately	PLSTMG33	Drive pulse timing setting 33	Set to 001Fh
3288h	0288h	[7:0]					
3289h	0289h	[7:0]					
328Ch	028Ch	[7:0]	0017h	immediately	PLSTMG35	Drive pulse timing setting 35	Set to 0013h
328Dh	028Dh	[7:0]					
328Eh	028Eh	[7:0]					
328Fh	028Fh	[7:0]	0000h	immediately	PLSTMG36	Drive pulse timing setting 36	Set to 001Fh
3290h	0290h	[7:0]					
3291h	0291h	[7:0]					
32AEh	02AEh	[7:0]	01h	immediately	PLSTMG38	Drive pulse timing setting 38	Set to 00h
32AFh	02AFh	[7:0]	01h	immediately	PLSTMG39	Drive pulse timing setting 39	Set to 00h
32CAh	02CAh	[7:0]	006Dh	*2	PLSTMG40	Drive pulse timing setting 40	Set to 005Ah
32CBh	02CBh	[7:0]					
332Ch	032Ch	[7:0]					
332Dh	032Dh	[7:0]	00FFh	immediately	PSSLVS1	Low Power Consumption Period Length 1	Setting range is shown in "Description of Registers"
332Fh	032Fh	[7:0]	02h	immediately	PLSTMG41	Drive pulse timing setting 41	Set to 00h
334Ah	034Ah	[7:0]	00FFh	immediately	PSSLVS2	Low Power Consumption Period Length 2	Setting range is shown in "Description of Registers"
334Bh	034Bh	[7:0]					
334Ch	034Ch	[7:0]					
335Ah	035Ah	[7:0]	008Ch	immediately	PLSTMG09	Drive pulse timing setting 09	Set to 01h
335Bh	035Bh	[7:0]					
335Eh	035Eh	[7:0]					
335Fh	035Fh	[7:0]	0069h	immediately	PLSTMG43	Drive pulse timing setting 43	Set to 0079h
3360h	0360h	[7:0]					
3361h	0361h	[7:0]					
336Ah	036Ah	[7:0]	0069h	immediately	PLSTMG44	Drive pulse timing setting 44	Set to 0056h
336Bh	036Bh	[7:0]					
336Dh	036Dh	[7:0]					
33D6h	03D6h	[7:0]	007Dh	immediately	PLSTMG45	Drive pulse timing setting 45	Set to 006Ah
33D7h	03D7h	[7:0]					
33D8h	03D8h	[7:0]					
340Ch	040Ch	[7:0]	008Ch	immediately	PLSTMG46	Drive pulse timing setting 46	Set to 0056h
340Dh	040Dh	[7:0]					
340Eh	040Eh	[7:0]					
3448h	0448h	[7:0]	0081h	immediately	PLSTMG47	Drive pulse timing setting 47	Set to 0079h
3449h	0449h	[7:0]					
348Eh	048Eh	[7:0]					
348Fh	048Fh	[7:0]	0091h	immediately	PLSTMG48	Drive pulse timing setting 48	Set to 006Eh
3492h	0492h	[7:0]					
34C4h	04C4h	[7:0]					
34C5h	04C5h	[7:0]	006Dh	*2	PLSTMG49	Drive pulse timing setting 49	Set to 007Eh
3506h	0506h	[7:0]					
3507h	0507h	[7:0]					
350Ch	050Ch	[7:0]	0069h	immediately	PLSTMG50	Drive pulse timing setting 50	Set to 006Fh
350Dh	050Dh	[7:0]					
350Eh	050Eh	[7:0]					
350Fh	050Fh	[7:0]	006Bh	immediately	PLSTMG51	Drive pulse timing setting 51	Set to 11h
3549h	0549h	[7:0]					
355Dh	055Dh	[7:0]					
355Eh	055Eh	[7:0]	006Dh	*2	PLSTMG52	Drive pulse timing setting 52	Set to 005Ah
3574h	0574h	[7:0]					
3575h	0575h	[7:0]					
3506h	0506h	[7:0]	0069h	immediately	PLSTMG53	Drive pulse timing setting 53	Set to 0056h
3507h	0507h	[7:0]					
350Ch	050Ch	[7:0]					
350Dh	050Dh	[7:0]	0069h	immediately	PLSTMG54	Drive pulse timing setting 54	Set to 0056h
350Eh	050Eh	[7:0]					
350Fh	050Fh	[7:0]					
3549h	0549h	[7:0]	006Bh	immediately	PLSTMG55	Drive pulse timing setting 55	Set to 0058h
355Dh	055Dh	[7:0]					
355Eh	055Eh	[7:0]					
3574h	0574h	[7:0]	0069h	immediately	PLSTMG56	Drive pulse timing setting 56	Set to 04h
3575h	0575h	[7:0]					
357Fh	057Fh	[7:0]					
3580h	0580h	[7:0]	05h	immediately	PLSTMG57	Drive pulse timing setting 57	Set to 03h
3581h	0581h	[7:0]					
3583h	0583h	[7:0]					
3574h	0574h	[7:0]	01h	immediately	PLSTMG58	Drive pulse timing setting 58	Set to 03h
3575h	0575h	[7:0]					
357Fh	057Fh	[7:0]					
357Fh	057Fh	[7:0]	0069h	immediately	PLSTMG59	Drive pulse timing setting 59	Set to 0056h
3580h	0580h	[7:0]					
3581h	0581h	[7:0]					
3583h	0583h	[7:0]	01h	immediately	PLSTMG60	Drive pulse timing setting 60	Set to 01h
3574h	0574h	[7:0]					
3575h	0575h	[7:0]					
357Fh	057Fh	[7:0]	08h	immediately	MDSEL11	Mode select 11	Set the value according to each readout mode register setting.
3580h	0580h	[7:0]					
3581h	0581h	[7:0]					
3583h	0583h	[7:0]	05h	immediately	MDSEL12	Mode select 12	Set the value according to each readout mode register setting.
3574h	0574h	[7:0]					
3575h	0575h	[7:0]					
357Fh	057Fh	[7:0]	02h	immediately	MDSEL13	Mode select 13	Set the value according to each readout mode register setting.
3580h	0580h	[7:0]					
3581h	0581h	[7:0]					
3583h	0583h	[7:0]	51h	immediately	MDSEL14	Mode select 14	Set the value according to each readout mode register setting.
3574h	0574h	[7:0]					
3575h	0575h	[7:0]					
357Fh	057Fh	[7:0]	00h	*1	PLSTMG60	Drive pulse timing setting 60	Set to 01h
3580h	0580h	[7:0]					
3581h	0581h	[7:0]					

Address		Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2 (I ² C)	SLVS-E C						
35B6h	05B6h	[7:0]	00FFh	immediately	PSSLVS3	Low Power Consumption Period Length 3	Setting range is shown in "Description of Registers"
35B7h	05B7h	[7:0]					
35B8h	05B8h	[7:0]					
35B9h	05B9h	[7:0]					
35D0h	05D0h	[7:0]	0071h	immediately	PLSTMG61	Drive pulse timing setting 61	Set to 005Eh
35D1h	05D1h	[7:0]					
35D4h	05D4h	[7:0]					
35D5h	05D5h	[7:0]					
35E5h	05E5h	[1:0]	0h	immediately	CLKDIVEN	Clock divide enable	Refer to the "Standby Cancel Sequence"
		[2]	0h			—	Set the default value.
		[3]	0h	immediately	SYSCLEN	System clock enable	Refer to the "Standby Cancel Sequence"
		[7:4]	9h			—	Set the default value.
3600h	0600h	[7:0]	0090h	immediately	MDSEL16	Mode select 16	Set the value according to each readout mode register setting.
3601h	0601h	[7:0]					
366Ah	066Ah	[7:0]					
366Bh	066Bh	[7:0]					
366Ch	066Ch	[7:0]	10h	immediately	PLSTMG63	Drive pulse timing setting 63	Set to 1Ah
366Dh	066Dh	[7:0]	0Eh	immediately	PLSTMG64	Drive pulse timing setting 64	Set to 16h
366Eh	066Eh	[7:0]	0Ch	immediately	PLSTMG65	Drive pulse timing setting 65	Set to 10h
366Fh	066Fh	[7:0]	0Ah	immediately	PLSTMG66	Drive pulse timing setting 66	Set to 09h
3670h	0670h	[7:0]	08h	immediately	PLSTMG67	Drive pulse timing setting 67	Set to 00h
3671h	0671h	[7:0]	06h	immediately	PLSTMG68	Drive pulse timing setting 68	Set to 00h
3672h	0672h	[7:0]	04h	immediately	PLSTMG69	Drive pulse timing setting 69	Set to 00h
3673h	0673h	[7:0]	02h	immediately	PLSTMG70	Drive pulse timing setting 70	Set to 00h
3674h	0674h	[7:0]	0400h	immediately	PLSTMG73	Drive pulse timing setting 73	Set to 0383h
3675h	0675h	[7:0]					
3676h	0676h	[7:0]					
3677h	0677h	[7:0]					
3678h	0678h	[7:0]	052Ch	immediately	PLSTMG74	Drive pulse timing setting 74	Set to 0400h
3679h	0679h	[7:0]					
367Ah	067Ah	[7:0]					
367Bh	067Bh	[7:0]					
367Ch	067Ch	[7:0]	0600h	immediately	PLSTMG75	Drive pulse timing setting 75	Set to 052Ch
367Dh	067Dh	[7:0]					
367Eh	067Eh	[7:0]					
367Fh	067Fh	[7:0]					
3680h	0680h	[7:0]	0700h	immediately	PLSTMG76	Drive pulse timing setting 76	Set to 0600h
3681h	0681h	[7:0]					
3682h	0682h	[7:0]					
3683h	0683h	[7:0]					
3684h	0684h	[7:0]	07A6h	immediately	PLSTMG78	Drive pulse timing setting 78	Set to 074Bh
3685h	0685h	[7:0]					
3686h	0686h	[7:0]					
3687h	0687h	[7:0]					
3688h	0688h	[7:0]	0004h	immediately	PLSTMG101	Drive pulse timing setting 101	Set to 0000h
3689h	0689h	[7:0]					
3690h	0690h	[7:0]					
3691h	0691h	[7:0]					
3692h	0692h	[7:0]	000Ah	immediately	PLSTMG79	Drive pulse timing setting 79	Set to 0027h
3693h	0693h	[7:0]					
3694h	0694h	[7:0]					
3695h	0695h	[7:0]					
3696h	0696h	[7:0]	0014h	immediately	PLSTMG80	Drive pulse timing setting 80	Set to 0065h
3697h	0697h	[7:0]					
3698h	0698h	[7:0]					
3699h	0699h	[7:0]					
36A0h	06A0h	[7:0]	000Ah	immediately	PLSTMG81	Drive pulse timing setting 81	Set to 004Fh
36A1h	06A1h	[7:0]					
36A2h	06A2h	[7:0]					
36A3h	06A3h	[7:0]					
36A4h	06A4h	[7:0]	0014h	immediately	PLSTMG82	Drive pulse timing setting 82	Set to 00A1h
36A5h	06A5h	[7:0]					
36A6h	06A6h	[7:0]					
36A7h	06A7h	[7:0]					
36B0h	06B0h	[7:0]	0001h	*2	PSSLVS0	Low Power Consumption Period Length 0	Setting range is shown in "Description of Registers"
36B1h	06B1h	[7:0]					
36B2h	06B2h	[7:0]					
36B3h	06B3h	[7:0]					
36B4h	06B4h	[7:0]	0000h	immediately	PLSTMG102	Drive pulse timing setting 102	Set to 0001h
36B5h	06B5h	[7:0]					
36B6h	06B6h	[7:0]					
36B7h	06B7h	[7:0]					
36B8h	06B8h	[7:0]	0000h	immediately	PLSTMG103	Drive pulse timing setting 103	Set to 0001h
36B9h	06B9h	[7:0]					
36BAh	06BAh	[7:0]					
36BBh	06BBh	[7:0]					
36BC	06BC	[7:0]	0000h	immediately	PLSTMG104	Drive pulse timing setting 104	Set to 0001h
36BD	06BD	[7:0]					
36BE	06BE	[7:0]					
36BF	06BF	[7:0]					
36C0	06C0	[7:0]	00h	immediately	PLSTMG105	Drive pulse timing setting 105	Set to 01h
36C1	06C1	[7:0]					
36C2	06C2	[7:0]					
36C3	06C3	[7:0]					
36C4	06C4	[7:0]	00h	immediately	PLSTMG106	Drive pulse timing setting 106	Set to 01h
36C5	06C5	[7:0]					
36C6	06C6	[7:0]					
36C7	06C7	[7:0]					
36C8	06C8	[7:0]	00h	immediately	PLSTMG107	Drive pulse timing setting 107	Set to 01h
36C9	06C9	[7:0]					
36CA	06CA	[7:0]					
36CB	06CB	[7:0]					
378Ch	078Ch	[0]	0h	immediately	EBDDATAEN	0h: Without embedded data insertion	Setting range: 0h to 1h
		[7:1]	00h			1h: With embedded data insertion	Set the default value.
382Bh	082Bh	[7:0]	79h	immediately	PLSTMG83	Drive pulse timing setting 83	Set to 68h
3846h	0846h	[7:0]	0000h	*1	MDSEL9	Mode select 9	Set the value according to each readout mode register setting.
3847h	0847h	[7:0]					
384Ah	084Ah	[7:0]					
384Bh	084Bh	[7:0]					
384Ch	084Ch	[7:0]	0000h	*1	MDSEL10	Mode select 10	Set the value according to each readout mode register setting.
384Dh	084Dh	[7:0]					
384Eh	084Eh	[7:0]					
384Fh	084Fh	[7:0]					
3C00h	0C00h	[7:0]	00h	immediately	PLSTMG84	Drive pulse timing setting 84	Set to 01h
3C01h	0C01h	[7:0]	00h	immediately	PLSTMG85	Drive pulse timing setting 85	Set to 01h

1. Description of Register

Total Standby Control (CSI-2 and SLVS-EC)

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY to "1h".

(Standby mode is established immediately after reset.)

The serial communication block operates even in standby mode, so standby mode can be canceled by setting "0h" in the STANDBY register.

STANDBY Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
STANDBY	3000h	0000h	[0]	0h	Normal operation
				1h	Overall standby

Digital Circuit Standby Control (CSI-2 and SLVS-EC)

When power-on, set the digital circuit standby control register STBLOGIC according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBLOGIC Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
STBLOGIC	3000h	0000h	[1]	0h	Normal operation
				1h	Digital circuit standby other than serial communications block

Frequency Demultiplier Standby Control (CSI-2 and SLVS-EC)

When power-on, set the frequency demultiplier standby control register STBDV according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBDV Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
STBDV	3000h	0000h	[4]	0h	Normal operation
				1h	Frequency demultiplier standby

Clamp Reset (CSI-2 and SLVS-EC)

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST. Make this setting according to the recommended sequence during power-on or when canceling standby mode.

This register automatically returns to "0h" after the reset process, so there is no need to write "0h".

CLPSQRST Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
CLPSQRST	3001h	0001h	[4]	Changed from 0h to 1h	Resets the internal clamp circuit operation status

Input Frequency Setting (CSI-2 and SLVS-EC)

The input clock frequency can be set arbitrarily by setting input clock setting register PLRD1, PLRD2, PLRD3, PLRD4, PLRD10, PLRD11, PLRD12, PLRD13, PLRD14 and PLRD15.

Set this registers according to the recommended sequence during power-on or when canceling standby mode.

Input Frequency Setting Registers

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Function
PLRD10 [7:0]	311Fh	011Fh	[7:0]	Input clock frequency setting register
PLRD2 [7:0]	3122h	0122h	[7:0]	
PLRD11 [7:0]	3123h	0123h	[7:0]	
PLRD12 [7:0]	3124h	0124h	[7:0]	
PLRD13 [7:0]	3125h	0125h	[7:0]	
PLRD14 [7:0]	3127h	0127h	[7:0]	
PLRD3 [7:0]	3129h	0129h	[7:0]	
PLRD4 [7:0]	312Ah	012Ah	[7:0]	
PLRD15 [7:0]	312Dh	012Dh	[7:0]	
PLRD1 [7:0]	31E8h	01E8h	[7:0]	
PLRD1 [15:8]	31E9h	01E9h	[7:0]	

PLRD1 to PLRD15 Setting (CSI-2)

		Register value									
		PLRD 1	PLRD 2	PLRD 3	PLRD 4	PLRD 10	PLRD 11	PLRD 12	PLRD 13	PLRD 14	PLRD 15
Input clock frequency [MHz] ^{*1}	6	0120h	00h	90h	00h	00h	00h	00h	01h	02h	02h
	12	0120h	01h	90h	01h						
	18	00C0h	01h	60h	01h						
	24	0120h	02h	90h	02h						

^{*1} Consult your Sony sales representative concerning other input frequency settings.

PLRD1 to PLRD15 Setting (SLVS-EC)

		Register value									
		PLRD 1	PLRD 2	PLRD 3	PLRD 4	PLRD 10	PLRD 11	PLRD 12	PLRD 13	PLRD 14	PLRD 15
Input clock frequency [MHz]	72	0010h	00h	0Ch	00h	01h	01h	01h	00h	06h	03h

Digital Black Level Offset (CSI-2 and SLVS-EC)

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL.

Note that the offset unit changes according to the readout drive mode.

When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits. When the output data length is 14-bit output, increasing the register setting value by 1h increases the black level by 16 digits.

BLKLEVEL Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
BLKLEVEL [7:0]	3042h	0042h	[7:0]	00h to FFh	Digital black level offset setting

Analog Gain (CSI-2 and SLVS-EC)

The analog gain value can be set by setting the analog gain register PGC. Set the lower 8 bits and the upper 3 bits, for total of 11 bits.

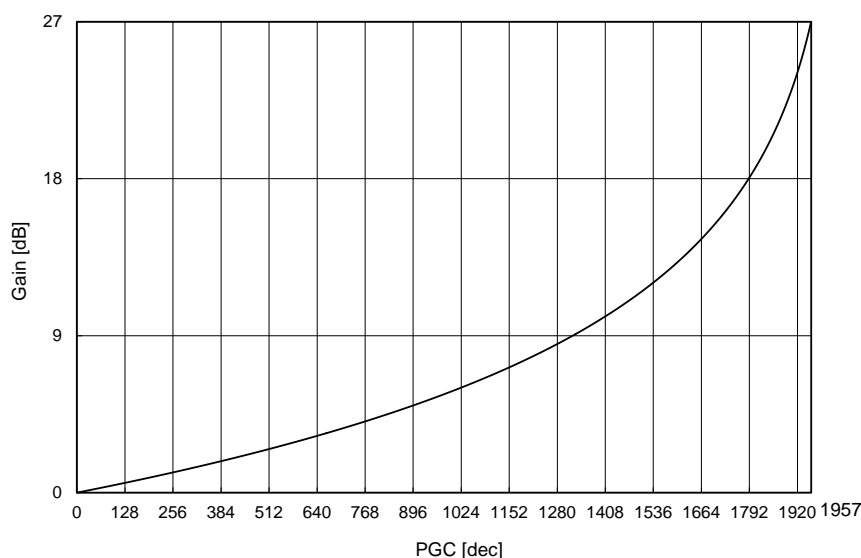
PGC Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
PGC [7:0]	300Ah	000Ah	[7:0]	0h to 7A5h (0d to 1957d)	Analog gain setting
PGC [10:8]	300Bh	000Bh	[2:0]		

In addition, the figure below shows the relationship between the register setting value and the gain value. When the register setting value is "0h (0d)", the gain value is 0 dB (minimum settable value), and when "7A5h (1957d)", the gain value is approximately 27 dB (maximum settable value).

Relation Formula

$$\text{Gain [dB]} = -20\log\{(2048 - \text{PGC [10:0]}) / 2048\}$$



Relationship between Register Setting Value and Set Gain Value

Digital Gain (CSI-2 and SLVS-EC)

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN.

DGAIN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
DGAIN [3:0]	3012h	0012h	[3:0]	0h	Digital gain setting value = 0 dB
				1h	Digital gain setting value = +6 dB
				2h	Digital gain setting value = +12 dB
				3h	Digital gain setting value = +18 dB
				Others	Prohibited

Conversion Gain (CSI-2 and SLVS-EC)

The conversion gain can be switched from low to high by the conversion gain switching register MCOVGAIN.

MCOVGAIN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
MCOVGAIN	3092h	0092h	[0]	0h	Conversion gain low
				1h	Conversion gain high

When using conversion gain high (MCOVGAIN=1), there is following restriction on setting range of analog gain,

Conversion gain switching	A/D conversion bits	Readout mode No.	Setting range of register PGC	Setting range of analog gain [dB]
MCOVGAIN=0	—	—	0h to 7A5h	0 to 27
MCOVGAIN=1	14	0	4D8h to 7A5h	8.07 to 27
	12	1, 1A, 1B, 3, 4	4A5h to 7A5h	7.54 to 27
	10	2, 2A, 5 to 11	608h to 7A5h	12.17 to 27

Followings are other notations when changing conversion gain by the register.

1. Power consumptions not vary with the conversion gain principally.
(But there can be analog/digital power consumption change by the change of output value.)
2. Saturation signal gets smaller according to MCOVG in "Image Sensor Characteristics" on page 31.
3. Noises in dark condition don't change principally.
So usually set MCOVGAIN=0→1 makes S/N ratio higher in according to MCOVG, but please confirm this characteristics in your environment since S/N ratio cannot be guaranteed.

Vertical Arbitrary Cropping (CSI-2 and SLVS-EC)

Arbitrary cropping in vertical direction can be enabled by setting vertical arbitrary cropping enable register VWIDCUTEN, and arbitrary cropping in vertical direction can be performed by designating cropping position of vertical direction to setting cropping width of vertical direction register VWINPOS and VWIDCUT. See "Vertical Arbitrary Cropping Function" on pages 90 to 92 and 128 to 130 for details.

VWIDCUTEN, VWIDCUT, VWINPOS Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Function
VWIDCUTEN	30DDh	00DDh	[0]	Vertical arbitrary cropping enable
VWIDCUT [7:0]	30DEh	00DEh	[7:0]	Width of vertical arbitrary cropping
VWIDCUT [13:8]	30DFh	00DFh	[5:0]	
VWINPOS [7:0]	30E0h	00E0h	[7:0]	Start position of vertical arbitrary cropping (two's complement)
VWINPOS [13:8]	30E1h	00E1h	[5:0]	

Vertical Direction Readout Inversion (CSI-2 and SLVS-EC)

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV. See "Optical Black Array and Readout Scan Direction" for details of readout image.

MDVREV Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
MDVREV	3017h	0017h	[0]	0h	Vertical direction normal readout
				1h	Vertical direction inversion readout

Horizontal Arbitrary Cropping (CSI-2 and SLVS-EC)

Arbitrary cropping in horizontal direction can be enabled by setting horizontal arbitrary cropping enable register HTRIMMING_EN, and arbitrary cropping in horizontal direction can be performed by designating cropping position of horizontal direction to setting cropping position of horizontal direction register HTRIMMING_START and HTRIMMING_END. See "Horizontal Arbitrary Cropping Function" on pages 93 to 94 and 131 to 132 for details.

HTRIMMING_EN, HTRIMMING_START, HTRIMMING_END Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Function
HTRIMMING_EN	3035h	0035h	[0]	Horizontal arbitrary cropping enable
HTRIMMING_START [7:0]	3036h	0036h	[7:0]	Horizontal cropping start position
HTRIMMING_START [13:8]	3037h	0037h	[5:0]	
HTRIMMING_END [7:0]	3038h	0038h	[7:0]	Horizontal cropping end position +1
HTRIMMING_END [13:8]	3039h	0039h	[5:0]	

Horizontal Drive Period Length and Vertical Drive Period Length (CSI-2 only)

When using CSI-2, Horizontal drive period length (Unit: 72MHz clock) and vertical drive period length (Unit: horizontal drive period) can be set by horizontal drive period length setting register HMAX and vertical drive period length setting register VMAX.

HMAX, VMAX Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Function
VMAX [7:0]	30A9h	—	[7:0]	Vertical drive period length (Unit: horizontal drive period)
VMAX [15:8]	30AAh	—	[7:0]	
VMAX [19:16]	30ABh	—	[3:0]	
HMAX [7:0]	30ACh	—	[7:0]	Horizontal drive period length (Unit: 72MHz clock)
HMAX [15:8]	30ADh	—	[7:0]	

Calculating formula of vertical drive period (1 frame) is shown below.

$$\text{Vertical drive period length [s]} = \text{VMAX value} \times (\text{SVR value} + 1) \times \text{HMAX value} / (72 \times 10^6)$$

See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on pages 79, 86, 105 and 121 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Low Power Consumption Period Length

Register PSSLVs0 to 4 enables adjustment of low power consumption period length while readout. To maximize power saving set calculated value from following constant every time when changing readout mode or VMAX (XVS period length).

$$\begin{aligned}
 1V &= \text{VMAX} \times (\text{SVR value} + 1) \\
 V_{\text{BLK}} &= 1V - \text{minimum XVS period} \quad (\text{SLVS-EC}) \\
 &= 1V - \text{minimum VMAX setting} \quad (\text{CSI-2})
 \end{aligned}$$

Set 0h to these registers when no adjustment is used or V_{BLK} is too small and some of setting value cannot be calculated.

Low Power Consumption Period Length Setting

Register Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Setting Value
PSSLVs1[7:0]	332Ch	032Ch	[7:0]	V_{BLK}
PSSLVs1[15:8]	332Dh	032Dh	[7:0]	
PSSLVs2[7:0]	334Ah	034Ah	[7:0]	V_{BLK}
PSSLVs2[15:8]	334Bh	034Bh	[7:0]	
PSSLVs3[7:0]	35B6h	05B6h	[7:0]	V_{BLK}
PSSLVs3[15:8]	35B7h	05B7h	[7:0]	
PSSLVs4[7:0]	35B8h	05B8h	[7:0]	$V_{\text{BLK}} - 5h$
PSSLVs4[15:8]	35B9h	05B9h	[7:0]	
PSSLVs0[7:0]	36BCh	06BCh	[7:0]	V_{BLK}
PSSLVs0[15:8]	36BDh	06BDh	[7:0]	

For example, when SLVS-EC output is used, for readout mode No.2 with 1 XVS = 1155 [XHS] and SVR=1, calculation result is as follows:

$$\begin{aligned}
 1V &= 1155 \times (1+1) = 2310 \\
 V_{\text{BLK}} &= 2310 - 1107 = 1203
 \end{aligned}$$

Readout Drive Mode (CSI-2 and SLVS-EC)

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL1 to 15, VCUTMODE, HMAX, VMAX, OPB_SIZE_V, WRITE_VSIZE, Y_OUT_SIZE, PSSLVs0 to 4 and HCOUNT1 to 2. When changing the mode, make the setting according to “Register Settings for Each Readout Drive Mode” on pages 62 to 67.

Readout Drive Pulse Timing (CSI-2 and SLVS-EC)

When power-on, set the readout drive pulse timing registers, PLSTMG09 to 104 according to the standby cancel sequence.

PLSTMG Setting (CSI-2 / SLVS-EC)

Register Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Setting Value
PLSTMG11	3047h	0047h	[7:0]	01h
PLSTMG12	304Eh	004Eh	[7:0]	0Bh
PLSTMG13	304Fh	004Fh	[7:0]	24h
PLSTMG14	3062h	0062h	[7:0]	25h
PLSTMG15	3064h	0064h	[7:0]	78h
PLSTMG16	3065h	0065h	[7:0]	33h
PLSTMG17	3067h	0067h	[7:0]	71h
PLSTMG18	3088h	0088h	[7:0]	75h
PLSTMG19[7:0]	308Ah	008Ah	[7:0]	0109h
PLSTMG19[15:8]	308Bh	008Bh	[7:0]	
PLSTMG20	308Ch	008Ch	[7:0]	61h
PLSTMG10	3146h	0146h	[7:0]	00h
PLSTMG21[7:0]	3234h	0234h	[7:0]	0032h
PLSTMG21[15:8]	3235h	0235h	[7:0]	
PLSTMG22[7:0]	3248h	0248h	[7:0]	00BCh
PLSTMG22[15:8]	3249h	0249h	[7:0]	
PLSTMG23[7:0]	3250h	0250h	[7:0]	00BCh
PLSTMG23[15:8]	3251h	0251h	[7:0]	
PLSTMG24[7:0]	3258h	0258h	[7:0]	00BCh
PLSTMG24[15:8]	3259h	0259h	[7:0]	
PLSTMG25[7:0]	3260h	0260h	[7:0]	00BCh
PLSTMG25[15:8]	3261h	0261h	[7:0]	
PLSTMG26[7:0]	3274h	0274h	[7:0]	0013h
PLSTMG26[15:8]	3275h	0275h	[7:0]	
PLSTMG27[7:0]	3276h	0276h	[7:0]	001Fh
PLSTMG27[15:8]	3277h	0277h	[7:0]	
PLSTMG28[7:0]	3278h	0278h	[7:0]	0030h
PLSTMG28[15:8]	3279h	0279h	[7:0]	
PLSTMG29[7:0]	327Ch	027Ch	[7:0]	0013h
PLSTMG29[15:8]	327Dh	027Dh	[7:0]	
PLSTMG30[7:0]	327Eh	027Eh	[7:0]	001Fh
PLSTMG30[15:8]	327Fh	027Fh	[7:0]	
PLSTMG31[7:0]	3280h	0280h	[7:0]	0030h
PLSTMG31[15:8]	3281h	0281h	[7:0]	
PLSTMG32[7:0]	3284h	0284h	[7:0]	0013h
PLSTMG32[15:8]	3285h	0285h	[7:0]	
PLSTMG33[7:0]	3286h	0286h	[7:0]	001Fh
PLSTMG33[15:8]	3287h	0287h	[7:0]	
PLSTMG34[7:0]	3288h	0288h	[7:0]	0030h
PLSTMG34[15:8]	3289h	0289h	[7:0]	
PLSTMG35[7:0]	328Ch	028Ch	[7:0]	0013h
PLSTMG35[15:8]	328Dh	028Dh	[7:0]	
PLSTMG36[7:0]	328Eh	028Eh	[7:0]	001Fh
PLSTMG36[15:8]	328Fh	028Fh	[7:0]	
PLSTMG37[7:0]	3290h	0290h	[7:0]	0030h
PLSTMG37[15:8]	3291h	0291h	[7:0]	
PLSTMG38	32AEh	02AEh	[7:0]	00h
PLSTMG39	32AFh	02AFh	[7:0]	00h
PLSTMG40[7:0]	32CAh	02CAh	[7:0]	005Ah
PLSTMG40[15:8]	32CBh	02CBh	[7:0]	
PLSTMG41	332Fh	032Fh	[7:0]	00h
PLSTMG09	334Ch	034Ch	[7:0]	01h
PLSTMG43[7:0]	335Ah	035Ah	[7:0]	0079h
PLSTMG43[15:8]	335Bh	035Bh	[7:0]	
PLSTMG44[7:0]	335Eh	035Eh	[7:0]	0056h
PLSTMG44[15:8]	335Fh	035Fh	[7:0]	
PLSTMG45[7:0]	3360h	0360h	[7:0]	006Ah
PLSTMG45[15:8]	3361h	0361h	[7:0]	
PLSTMG46[7:0]	336Ah	036Ah	[7:0]	0056h
PLSTMG46[15:8]	336Bh	036Bh	[7:0]	
PLSTMG47[7:0]	33D6h	03D6h	[7:0]	0079h
PLSTMG47[15:8]	33D7h	03D7h	[7:0]	
PLSTMG48[7:0]	340Ch	040Ch	[7:0]	006Eh
PLSTMG48[15:8]	340Dh	040Dh	[7:0]	
PLSTMG49[7:0]	3448h	0448h	[7:0]	007Eh
PLSTMG49[15:8]	3449h	0449h	[7:0]	

Register Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Setting Value
PLSTMG50[7:0]	348Eh	048Eh	[7:0]	006Fh
PLSTMG50[15:8]	348Fh	048Fh	[7:0]	
PLSTMG51	3492h	0492h	[7:0]	11h
PLSTMG52[7:0]	34C4h	04C4h	[7:0]	005Ah
PLSTMG52[15:8]	34C5h	04C5h	[7:0]	
PLSTMG53[7:0]	3506h	0506h	[7:0]	0056h
PLSTMG53[15:8]	3507h	0507h	[7:0]	
PLSTMG54[7:0]	350Ch	050Ch	[7:0]	0056h
PLSTMG54[15:8]	350Dh	050Dh	[7:0]	
PLSTMG55[7:0]	350Eh	050Eh	[7:0]	0058h
PLSTMG55[15:8]	350Fh	050Fh	[7:0]	
PLSTMG56	3549h	0549h	[7:0]	04h
PLSTMG57	355Dh	055Dh	[7:0]	03h
PLSTMG58	355Eh	055Eh	[7:0]	03h
PLSTMG59[7:0]	3574h	0574h	[7:0]	0056h
PLSTMG59[15:8]	3575h	0575h	[7:0]	
PLSTMG60	3587h	0587h	[7:0]	01h
PLSTMG61[7:0]	35D0h	05D0h	[7:0]	005Eh
PLSTMG61[15:8]	35D1h	05D1h	[7:0]	
PLSTMG62[7:0]	35D4h	05D4h	[7:0]	0063h
PLSTMG62[15:8]	35D5h	05D5h	[7:0]	
PLSTMG63	366Ah	066Ah	[7:0]	1Ah
PLSTMG64	366Bh	066Bh	[7:0]	16h
PLSTMG65	366Ch	066Ch	[7:0]	10h
PLSTMG66	366Dh	066Dh	[7:0]	09h
PLSTMG67	366Eh	066Eh	[7:0]	00h
PLSTMG68	366Fh	066Fh	[7:0]	00h
PLSTMG69	3670h	0670h	[7:0]	00h
PLSTMG70	3671h	0671h	[7:0]	00h
PLSTMG73[7:0]	3676h	0676h	[7:0]	0383h
PLSTMG73[15:8]	3677h	0677h	[7:0]	
PLSTMG74[7:0]	3678h	0678h	[7:0]	0400h
PLSTMG74[15:8]	3679h	0679h	[7:0]	
PLSTMG75[7:0]	367Ah	067Ah	[7:0]	052Ch
PLSTMG75[15:8]	367Bh	067Bh	[7:0]	
PLSTMG76[7:0]	367Ch	067Ch	[7:0]	0600h
PLSTMG76[15:8]	367Dh	067Dh	[7:0]	
PLSTMG77[7:0]	367Eh	067Eh	[7:0]	0700h
PLSTMG77[15:8]	367Fh	067Fh	[7:0]	
PLSTMG78[7:0]	3680h	0680h	[7:0]	074Bh
PLSTMG78[15:8]	3681h	0681h	[7:0]	
PLSTMG79[7:0]	3690h	0690h	[7:0]	0027h
PLSTMG79[15:8]	3691h	0691h	[7:0]	
PLSTMG80[7:0]	3692h	0692h	[7:0]	0065h
PLSTMG80[15:8]	3693h	0693h	[7:0]	
PLSTMG81[7:0]	3694h	0694h	[7:0]	004Fh
PLSTMG81[15:8]	3695h	0695h	[7:0]	
PLSTMG82[7:0]	3696h	0696h	[7:0]	00A1h
PLSTMG82[15:8]	3697h	0697h	[7:0]	
PLSTMG83	382Bh	082Bh	[7:0]	68h
PLSTMG84	3C00h	0C00h	[7:0]	01h
PLSTMG85[7:0]	3C01h	0C01h	[7:0]	01h
PLSTMG101[7:0]	3686h	0686h	[7:0]	0000h
PLSTMG101[15:8]	3687h	0687h	[7:0]	
PLSTMG102[7:0]	36BEh	06BEh	[7:0]	0001h
PLSTMG102[15:8]	36BFh	06BFh	[7:0]	
PLSTMG103[7:0]	36C0h	06C0h	[7:0]	0001h
PLSTMG103[15:8]	36C1h	06C1h	[7:0]	
PLSTMG104[7:0]	36C2h	06C2h	[7:0]	0001h
PLSTMG104[15:8]	36C3h	06C3h	[7:0]	
PLSTMG105	36C4h	06C4h	[7:0]	01h
PLSTMG106	36C5h	06C5h	[7:0]	01h
PLSTMG107	36C6h	06C6h	[7:0]	01h

Global Timing Registers

When power-on, set the global timing registers tclkpost to tlp_x according to the standby cancel sequence.

Global Timing Registers (CSI-2)

Register Name	CSI-2 (I ² C) Address	Bit	Setting Value
tclkpost	3134h	[7:0]	Set to 00AFh
	3135h	[7:0]	
thszero	3136h	[7:0]	Set to 00C7h
	3137h	[7:0]	
thsprepare	3138h	[7:0]	Set to 007Fh
	3139h	[7:0]	
tclktrail	313Ah	[7:0]	Set to 006Fh
	313Bh	[7:0]	
thstrail	313Ch	[7:0]	Set to 006Fh
	313Dh	[7:0]	
tclkzero	313Eh	[7:0]	Set to 01CFh
	313Fh	[7:0]	
tclkprepare	3140h	[7:0]	Set to 0077h
	3141h	[7:0]	
tlp _x	3142h	[7:0]	Set to 005Fh
	3143h	[7:0]	

PLL Standby Control (CSI-2 and SLVS-EC)

When power-on, set the PLL standby control registers STBPL_IF and STBPL_AD according to the standby cancel sequence. These registers are valid only when STANDBY = 0h.

STBPL_IF and STBPL_AD Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Function
STBPL_IF	310Bh	010Bh	[0]	PLL standby control register for IF
STBPL_AD	310Bh	010Bh	[4]	PLL standby control register for AD

Master / Slave Switching Control (CSI-2 and SLVS-EC)

When power-on, set the master / slave switching control register MSTSLV according to the standby cancel sequence.

MSTSLV Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
MSTSLV	3033h	0033h	[5]	0h	Slave mode
				1h	Master mode

Embedded Data Output Setting (CSI-2 and SLVS-EC)

Sensor internal operation information (readout mode, shutter, gain and so on) can be output as embedded data using the register EBDDATAEN. When using CSI-2, these data are output in 2 lines just before user clamp area. And when using SLVS-EC, these data are output in 1 line just before user clamp area. See Readout Pixel Image Diagram of each mode for detailed output timing. And see “Embedded Data” on pages 74 and 104 for details of embedded data.

EBDDATAEN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
EBDDATAEN	378Ch	078Ch	[0]	0h	Without embedded data insertion
				1h	With embedded data insertion

CSI-2 Standby Control (CSI-2 only)

CSI-2 can be standby by CSI-2 standby register STBMPI.

STBMPI Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
STBMPI	3000h	—	[3]	0h	Normal operation
				1h	CSI-2 standby

Master Mode Operation Control (CSI-2 only)

When power-on, set the master mode operation control register XMSTA according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

XMSTA Setting

Name	CSI-2 Address	SLVS-EC Address	Bit	Register value	Function
XMSTA	3033h	—	[0]	0h	Master mode start
				1h	Master mode stop

TX Manual Reset (SLVS-EC only)

The training sequence can be performed manually by setting the register MDCHGRST.
This register automatically returns to "0h" after the training sequence, so there is no need to write "0h".

MDCHGRST Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
MDCHGRST	—	0001h	[0]	Change from 0h to 1h	Training sequence starts after communication period

Break Mode (SLVS-EC only)

XVS can be subsampled according to SVR. This XVS subsampling operation can be stopped and then restarted from the start of the exposure period using the break mode register SSBRK.
This register automatically returns to "0h" after the break process, so there is no need to write "0h".

SSBRK Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
SSBRK	—	0002h	[0]	Change from 0h to 1h	Interrupt enable

SLVS-EC I/F Output Lane Number Selecting (SLVS-EC only)

This sensor can set the number of output lanes according to the setting values of the lane number selecting register LANESEL. When changing the number of output lanes, the training sequence is performed.

LANESEL Setting (SLVS-EC only)

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
LANESEL [2:0]	—	0003h	[6:4]	0h	8 Lane
				1h	6 Lane
				2h	4 Lane
				3h	2 Lane
				4h	1 Lane
				Others	Prohibited

Number of Output Lanes Settings (SLVS-EC only)

LANESEL	Remarks	Lane No.							
		0	1	2	3	4	5	6	7
00h	8 Lane	Active	Active	Active	Active	Active	Active	Active	Active
10h	6 Lane	Active	Active	Active	Active	Active	Active	Hi-Z	Hi-Z
20h	4 Lane	Active	Active	Active	Active	Hi-Z	Hi-Z	Hi-Z	Hi-Z
30h	2 Lane	Active	Active	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
40h	1 Lane	Active	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Others	prohibited								

Payload Data ECC, CRC Setting (SLVS-EC only)

The registers ECCEN can set ECC option for payload data error correction. The registers CRCEN can set CRC option for data transfer error correction. ECCEN and CRCEN cannot be used together. And, change ECCEN or CRCEN value during initialize communication of standby cancel sequence.

See "SLVS-EC Specification" for details of payload data, ECC and CRC.

CRCEN Setting (SLVS-EC only)

Name	CSI-2 Address	SLVS-EC Address	Bit	Register value	Function
CRCEN	—	00F4h	[0]	0h	Without CRC insertion into packet footer
				1h	With CRC insertion into packet footer ECC option and CRCEN option cannot be used together

ECCEN Setting (SLVS-EC only)

Name	CSI-2 Address	SLVS-EC Address	Bit	Register value	Function
ECCEN	—	00F5h	[1:0]	0h	Without ECC insertion.
				1h	With ECC [parity 2 byte]. ECC option and CRCEN option cannot be used together
				2h	With ECC [parity 4 byte]. ECC option and CRCEN option cannot be used together
				3h	Prohibited

Attribute Register and PHY Control Code (SLVS-EC only)

Correspondence of attribute register and PHY control code in “SLVS-EC Specification” to this sensor's registers are shown below.

Attribute Register (SLVS-EC only)

Attribute Register	Register name	SLVS-EC Address [bit]	Description
Sync Symbol	PHY Control Code see Sync Code		
Deskew Symbol	PHY Control Code see Deskew Code		
Standby Symbol	PHY Control Code see Standby Code		
Sync Length	SYNC_LENGTH	0115h[7:0], 0116h[7:0], 0117h[7:0]	Sync code repeat count in training sequence Default: 007FFFh Setting range: 000001h to 007FFFh
Deskew Length	DESKEW_LENGTH	011Ah[7:0]	Deskew code repeat count in training sequence Default: 10h Setting range: 01h to FFh
Standby Length	STANDBY_LENGTH	0119h[7:0]	Standby code repeat count in standby sequence Default: 10h Setting range: 03h to FFh
Deskew Interval	DESKEW_INTERVAL	0118h[7:0]	Idle code repeat count between deskew code in training sequence Default: 10h Setting range: 03h to FFh
Initial Length	INIT_LENGTH	0114h[4:0]	Low output period during mode change and initialization Default: 0Ah Setting range: 01h to 10h
Idle Code	PHY Control Code see Idle Code		

PHY Control Code (SLVS-EC only)

PHY Control Code	Register name	SLVS-EC Address [bit]	Description	8b10b symbol configuration			
Idle Code	IDLE_CODE1	0072h[7:0]	Any symbol	IDLE CODE 1 (def D.00.0)	IDLE CODE 2 (def D.00.0)	IDLE CODE 3 (def D.00.0)	IDLE CODE 4 (def D.00.0)
		0073h[0]	0:D character 1:K character				
	IDLE_CODE2	0074h[7:0]	Any symbol				
		0075h[0]	0:D character 1:K character				
	IDLE_CODE3	0076h[7:0]	Any symbol				
		0077h[0]	0:D character 1:K character				
	IDLE_CODE4	0078h[7:0]	Any symbol				
		0079h[0]	0:D character 1:K character				
Start Code				K.28.5	K.27.7	K.28.2	K.27.7
End Code				K.28.5	K.29.7	K.30.7	K.29.7
Pad Code				K.23.7	K.28.4	K.28.6	K.28.3
Sync Code	SYNC_SYMBOL	006Eh[7:0]	Any symbol	K.28.5	SYNC CODE (def D.10.5)	←	←
		006Fh[0]	0:D character 1:K character				
Deskew Code	DESKEW_SYMBOL	0070h[7:0]	Any symbol	K.28.5	DESKEW CODE (def D.00.3)	←	←
		0071h[0]	0:D character 1:K character				
Standby Code	STANDBY_SYMBOL	00EAh[7:0]	Any symbol	K.28.5	STBY CODE (def D.03.0)	←	←
		00EBh[0]	0:D character 1:K character				

2. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below. These registers should be change according to the mode to use. Set the register to the following value.

2-1. When Using Aspect Ratio Approx. 17:9 (Approx. 9.07 M pixels)

Description of Register Setting for Readout Drive Modes 1 to 4 (CSI-2)

Address (12C)	Bit Assignment	Register Name	Readout mode No. ^{*1}													
			1	1A	1B	2	2A	3	4							
3004h	[7:0]	MDSEL1	1Ah	01h	02h	1Ah	01h	A8h	0Ah							
3005h	[7:0]	MDSEL2	06h	06h	06h	01h	01h	2Ah	26h							
3006h	[7:0]	MDSEL3	00h	00h	01h	00h	00h	00h	00h							
3007h	[7:0]	MDSEL4	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A1h: normal / A6h: inverted							
300Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)													
300Fh	[7:0]															
3019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted 00h													
	[7:1]															
302Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)													
302Dh	[7:0]															
3030h	[7:0]	MDSEL5	77h	77h	77h	77h	77h	77h	33h: normal / 66h: inverted							
3034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h	0h	0h							
	[7:1]		00h	00h	00h	00h	00h	00h	00h							
3035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h	1h	1h							
	[7:1]		00h	00h	00h	00h	00h	00h	00h							
3036h	[7:0]	HTRIMMING_ START	30h	30h	30h	30h	30h	30h	30h							
3037h	[5:0]															
	[7:6]		0h	0h	0h	0h	0h	0h	0h							
3038h	[7:0]	HTRIMMING_ END	1060h	1080h	0F50h	1060h	1080h	1080h	1080h							
3039h	[5:0]															
	[7:6]		0h	0h	0h	0h	0h	0h	0h							
3068h	[7:0]	MDSEL15	001Ah	001Ah	001Ah	0044h	0044h	001Ah	001Ah							
3069h	[7:0]															
3080h	[7:0]	MDSEL6	00h	01h	00h	00h	01h	00h	00h							
3081h	[7:0]	MDSEL7	01h	01h	01h	01h	01h	01h	00h							
3084h	[7:0]	HCOUNT1	Set the same value as HMAX													
3085h	[7:0]															
3086h	[7:0]															
3087h	[7:0]															
	[7:0]	HCOUNT2	Set the same value as HMAX													
30A8h	[7:0]															
30A9h	[7:0]															
30AAh	[7:0]															
	[3:0]	VMAX	Set vertical drive period length (Unit: HMAX ×72MHz clock) ^{*2}													
30ABh	[7:4]															
	[7:0]	HMAX	Set horizontal drive period length (Unit: 72MHz clock) ^{*2}													
30ADh	[7:0]															
30E2h	[7:0]	VCUTMODE	00h	00h	00h	00h	00h	02h	03h							
312Fh	[5:0]	OPB_SIZE_V	08h	08h	08h	08h	08h	04h	04h							
	[7:6]		0h													
3130h	[7:0]	WRITE_VSIZE	0888h	0888h	0888h	0888h	0888h	044Ch	044Ch							
3131h	[4:0]			0h												
	[7:5]			0h												
3132h	[7:0]	Y_OUT_SIZE	0880h	0880h	0880h	0880h	0880h	0448h	0448h							
3133h	[4:0]			0h												
	[7:5]		0h													
332Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.													
332Dh	[7:0]															
334Ah	[7:0]	PSSLVS2								See “Low Power Consumption Period Length” on page 54.						
334Bh	[7:0]															
357Fh	[7:0]	MDSEL11	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch							
3580h	[7:0]	MDSEL12	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah							
3581h	[7:0]	MDSEL13	08h	08h	08h	0Ah	0Ah	08h	08h							
3583h	[7:0]	MDSEL14	72h	72h	72h	75h	75h	72h	72h							
35B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.													
35B7h	[7:0]															
35B8h	[7:0]	PSSLVS4								See “Low Power Consumption Period Length” on page 54.						
35B9h	[7:0]															
3600h	[7:0]	MDSEL16	0090h	007Dh	0090h	0090h	007Dh	0090h	0090h							
3601h	[7:0]			See “Low Power Consumption Period Length” on page 54.												
36BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54.													
36BDh	[7:0]															
3846h	[7:0]	MDSEL9								0000h	0000h	0000h	0000h	0000h	0000h	0000h
3847h	[7:0]										0000h					
384Ah	[7:0]	MDSEL10	0000h	0000h	0000h	0000h	0000h	0000h	0000h							
384Bh	[7:0]			0000h												

Description of Register Setting for Readout Drive Modes 5 to 11 (CSI-2)

Address (i ² C)	Bit Assign- ment	Register Name	Readout mode No. ^{*1}							
			5	6	7	8	9	10	11	
3004h	[7:0]	MDSEL1	A8h	0Ah	0Dh	4Fh	11h	33h	15h	
3005h	[7:0]	MDSEL2	25h	41h	41h	35h	35h	35h	31h	
3006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h	38h	
3007h	[7:0]	MDSEL4	A0h: normal / A5h: inverted	A1h: normal / A6h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A1h: normal / A6h: inverted	
300Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)							Multiple of 8 -1
300Fh	[7:0]									
3019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted							
	[7:1]		00h							
302Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)							
302Dh	[7:0]									
3030h	[7:0]	MDSEL5	77h	33h: normal / 66h: inverted	77h	77h	77h	77h	55h	
3034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h	0h	0h	
	[7:1]		00h	00h	00h	00h	00h	00h	00h	
3035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h	1h	1h	
	[7:1]		00h	00h	00h	00h	00h	00h	00h	
3036h	[7:0]	HTRIMMING_ START	30h	30h	30h	30h	30h	30h	30h	
3037h	[5:0]									
	[7:6]		0h	0h	0h	0h	0h	0h	0h	
3038h	[7:0]	HTRIMMING_	1080h	1080h	1080h	1080h	1080h	1080h	1080h	
3039h	[5:0]	END								
	[7:6]		0h	0h	0h	0h	0h	0h	0h	
3068h	[7:0]	MDSEL15	0044h	0044h	0044h	0044h	0044h	0044h	0044h	
3069h	[7:0]									
3080h	[7:0]	MDSEL6	00h	00h	00h	00h	00h	00h	00h	
3081h	[7:0]	MDSEL7	01h	00h	01h	01h	01h	01h	00h	
3084h	[7:0]	HCOUNT1	Set the same value as HMAX							
3085h	[7:0]									
3086h	[7:0]	HCOUNT2	Set the same value as HMAX							
3087h	[7:0]									
30A8h	[7:0]	MDSEL8	02h	02h	02h	02h	02h	02h	02h	
30A9h	[7:0]	VMAX	Set vertical drive period length (Unit: HMAX × 72MHz clock) ^{*2}							
30AAh	[7:0]									
30ABh	[3:0]		0h							
	[7:4]									
30ACh	[7:0]	HMAX	Set horizontal drive period length (Unit: 72MHz clock) ^{*2}							
30ADh	[7:0]									
30E2h	[7:0]	VCUTMODE	02h	03h	04h	05h	06h	07h	08h	
312Fh	[5:0]	OPB_SIZE_V	04h	04h	04h	04h	04h	04h	04h	
	[7:6]		0h							
3130h	[7:0]	WRITE_VSIZE	044Ch	044Ch	044Ch	02E4h	02E4h	00FCh	00FAh	
3131h	[4:0]			0h						
	[7:5]		0h							
3132h	[7:0]	Y_OUT_SIZE	0448h	0448h	0448h	02E0h	02E0h	00F8h	00F6h	
3133h	[4:0]			0h						
	[7:5]		0h							
332Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.							
332Dh	[7:0]									
334Ah	[7:0]	PSSLVS2								
334Bh	[7:0]									
357Fh	[7:0]	MDSEL11	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	
3580h	[7:0]	MDSEL12	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	
3581h	[7:0]	MDSEL13	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	
3583h	[7:0]	MDSEL14	75h	75h	75h	75h	75h	75h	75h	
35B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.							
35B7h	[7:0]									
35B8h	[7:0]	PSSLVS4								
35B9h	[7:0]									
3600h	[7:0]	MDSEL16	0090h	0090h	0090h	0090h	0090h	0090h	0090h	
3601h	[7:0]									
36BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54.							
36BDh	[7:0]									
3846h	[7:0]	MDSEL9	0000h	0000h	006Ch	0000h	0028h	0032h	003Ch	
3847h	[7:0]									
384Ah	[7:0]	MDSEL10	0000h	0000h	0034h	0000h	003Ah	0020h	0034h	
384Bh	[7:0]									

^{*1} See "Readout Drive Modes" on pages 68 to 69 for details of readout mode No.

^{*2} See "Horizontal/Vertical Operation Period in Each Readout Drive Mode" on page 79 and "Frame Rate Adjustment" on page 80 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Description of Register Setting for Readout Drive Modes 1 to 5 (SLVS-EC)

Address (SLVS-EC)	Bit Assign- ment	Register Name	Readout mode No. ^{*1}						
			1	1A	2	2A	3	4	5
0003h	[3:0]		0h						
	[6:4]	LANESEL	1h	1h	0h	1h	2h	2h	1h
	[7]		0h						
0004h	[7:0]	MDSEL1	1Ah	01h	1Ah	01h	A8h	0Ah	A8h
0005h	[7:0]	MDSEL2	06h	06h	01h	01h	2Ah	26h	25h
0006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h	00h
0007h	[7:0]	MDSEL4	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A1h: normal / A6h: inverted	A0h: normal / A5h: inverted
000Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)						
000Fh	[7:0]								
0019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted 00h						
	[7:1]								
002Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)						
002Dh	[7:0]								
0030h	[7:0]	MDSEL5	77h	77h	77h	77h	77h	33h: normal / 66h: inverted	77h
0034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h	00h	00h
0035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h	1h	1h
	[7:1]		00h	00h	00h	00h	00h	00h	00h
0036h	[7:0]	HTRIMMING_	30h	30h	30h	30h	30h	30h	30h
0037h	[5:0]	START							
	[7:6]		0h	0h	0h	0h	0h	0h	0h
0038h	[7:0]	HTRIMMING_	1060h	1080h	1060h	1080h	1080h	1080h	1080h
0039h	[5:0]	END							
	[7:6]		0h	0h	0h	0h	0h	0h	0h
0068h	[7:0]	MDSEL15	001Ah	001Ah	0044h	0044h	001Ah	001Ah	0044h
0069h	[7:0]								
0080h	[7:0]	MDSEL6	00h	01h	00h	01h	00h	00h	00h
0081h	[7:0]	MDSEL7	01h	01h	01h	01h	01h	00h	01h
0084h	[7:0]	HCOUNT1	Set XHS period [INCK@72 MHz]						
0085h	[7:0]								
0086h	[7:0]	HCOUNT2	Set XHS period [INCK@72 MHz]						
0087h	[7:0]								
00A8h	[7:0]	MDSEL8	02h	02h	02h	02h	02h	02h	02h
00E2h	[7:0]	VCUTMODE	00h	00h	00h	00h	02h	03h	02h
032Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.						
032Dh	[7:0]								
034Ah	[7:0]	PSSLVS2							
034Bh	[7:0]								
057Fh	[7:0]	MDSEL11	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch
0580h	[7:0]	MDSEL12	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
0581h	[7:0]	MDSEL13	08h	08h	0Ah	0Ah	08h	08h	0Ah
0583h	[7:0]	MDSEL14	72h	72h	75h	75h	72h	72h	75h
05B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.						
05B7h	[7:0]								
05B8h	[7:0]	PSSLVS4							
05B9h	[7:0]								
0600h	[7:0]	MDSEL16	0090h	007Dh	0090h	007Dh	0090h	0090h	0090h
0601h	[7:0]								
06BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54						
06BDh	[7:0]								
0846h	[7:0]	MDSEL9	0000h	0000h	0000h	0000h	0000h	0000h	0000h
0847h	[7:0]								
084Ah	[7:0]	MDSEL10	0000h	0000h	0000h	0000h	0000h	0000h	0000h
084Bh	[7:0]								

Description of Register Setting for Readout Drive Modes 6 to 11 (SLVS-EC)

Address (SLVS-EC)	Bit Assign- ment	Register Name	Readout mode No. *1						
			6	7	8	9	10	11	
0003h	[3:0]		0h						
	[6:4]	LANESEL	2h	2h	2h	2h	3h	4h	
	[7]		0h						
0004h	[7:0]	MDSEL1	0Ah	0Dh	4Fh	11h	33h	15h	
0005h	[7:0]	MDSEL2	41h	41h	35h	35h	35h	31h	
0006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	38h	
0007h	[7:0]	MDSEL4	A1h: normal / A6h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A1h: normal / A6h: inverted	
000Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)						Multiple of 8 –1
000Fh	[7:0]								
0019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted						
	[7:1]		00h						
002Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)						
002Dh	[7:0]								
0030h	[7:0]	MDSEL5	33h: normal / 66h: inverted	77h	77h	77h	77h	55h	
0034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h	0h	
	[7:1]		00h	00h	00h	00h	00h	00h	
0035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h	1h	
	[7:1]		00h	00h	00h	00h	00h	00h	
0036h	[7:0]	HTRIMMING_	30h	30h	30h	30h	30h	30h	
0037h	[5:0]	START							
	[7:6]		0h	0h	0h	0h	0h	0h	
0038h	[7:0]	HTRIMMING_	1080h	1080h	1080h	1080h	1080h	1080h	
0039h	[5:0]	END							
	[7:6]		0h	0h	0h	0h	0h	0h	
0068h	[7:0]	MDSEL15	0044h	0044h	0044h	0044h	0044h	0044h	
0069h	[7:0]								
0080h	[7:0]	MDSEL6	00h	00h	00h	00h	00h	00h	
0081h	[7:0]	MDSEL7	00h	01h	01h	01h	01h	00h	
0084h	[7:0]	HCOUNT1	Set XHS period [INCK@72 MHz]						
0085h	[7:0]								
0086h	[7:0]	HCOUNT2	Set XHS period [INCK@72 MHz]						
0087h	[7:0]								
00A8h	[7:0]	MDSEL8	02h	02h	02h	02h	02h	02h	
00E2h	[7:0]	VCUTMODE	03h	04h	05h	06h	07h	08h	
032Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.						
032Dh	[7:0]								
034Ah	[7:0]	PSSLVS2							
034Bh	[7:0]								
057Fh	[7:0]	MDSEL11	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	
0580h	[7:0]	MDSEL12	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	
0581h	[7:0]	MDSEL13	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	
0583h	[7:0]	MDSEL14	75h	75h	75h	75h	75h	75h	
05B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.						
05B7h	[7:0]								
05B8h	[7:0]	PSSLVS4							
05B9h	[7:0]								
0600h	[7:0]	MDSEL16	0090h	0090h	0090h	0090h	0090h	0090h	
0601h	[7:0]								
06BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54.						
06BDh	[7:0]								
0846h	[7:0]	MDSEL9	0000h	006Ch	0000h	0028h	0032h	003Ch	
0847h	[7:0]								
084Ah	[7:0]	MDSEL10	0000h	0034h	0000h	003Ah	0020h	0034h	
084Bh	[7:0]								

*1 See "Readout Drive Modes" on pages 68 to 69 for details of readout mode No.

2-2. When Using Aspect Ratio 4:3 (Approx. 10.71 M pixels)

Description of Register Setting for Each Readout Drive Modes (CSI-2)

Address (I ² C)	Bit Assign- ment	Register Name	Readout mode No. ^{*1}				
			0	1	1A	7	10
3004h	[7:0]	MDSEL1	00h	00h	00h	0Ch	32h
3005h	[7:0]	MDSEL2	0Bh	06h	06h	41h	35h
3006h	[7:0]	MDSEL3	02h	02h	02h	02h	02h
3007h	[7:0]	MDSEL4	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted
300Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)				
300Fh	[7:0]						
3019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted				
	[7:1]		00h				
302Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)				
302Dh	[7:0]						
3030h	[7:0]	MDSEL5	77h	77h	77h	77h	77h
3034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h
	[7:1]		00h	00h	00h	00h	00h
3035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h
	[7:1]		00h	00h	00h	00h	00h
3036h	[7:0]	HTRIMMING_ START	30h	30h	30h	30h	30h
3037h	[5:0]						
	[7:6]		0h	0h	0h	0h	0h
3038h	[7:0]	HTRIMMING_ END	0F00h	0F00h	0F00h	0F00h	0F00h
3039h	[5:0]						
	[7:6]		0h	0h	0h	0h	0h
3068h	[7:0]	MDSEL15	0044h	001Ah	001Ah	0044h	0044h
3069h	[7:0]						
3080h	[7:0]	MDSEL6	00h	00h	01h	00h	00h
3081h	[7:0]	MDSEL7	01h	01h	01h	01h	01h
3084h	[7:0]	HCOUNT1	Set the same value as HMAX				
3085h	[7:0]						
3086h	[7:0]	HCOUNT2	Set the same value as HMAX				
3087h	[7:0]						
30A8h	[7:0]	MDSEL8	03h	02h	02h	02h	02h
30A9h	[7:0]	VMAX	Set vertical drive period length (Unit: HMAX × 72MHz clock) ^{*2}				
30AAh	[7:0]						
30ABh	[3:0]						
	[7:4]		0h				
30ACh	[7:0]	HMAX	Set horizontal drive period length (Unit: 72MHz clock) ^{*2}				
30ADh	[7:0]						
30E2h	[7:0]	VCUTMODE	00h	00h	00h	04h	07h
312Fh	[5:0]	OPB_SIZE_V	10h	10h	10h	04h	04h
	[7:6]		0h				
3130h	[7:0]	WRITE_VSIZE	0B18h	0B18h	0B18h	0580h	0140h
3131h	[4:0]		0h				
	[7:5]						
3132h	[7:0]	Y_OUT_SIZE	0B08h	0B08h	0B08h	057Ch	013Ch
3133h	[4:0]		0h				
	[7:5]						
332Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.				
332Dh	[7:0]						
334Ah	[7:0]	PSSLVS2					
334Bh	[7:0]						
357Fh	[7:0]	MDSEL11	0Ah	0Ch	0Ch	0Ch	0Ch
3580h	[7:0]	MDSEL12	09h	0Ah	0Ah	0Ah	0Ah
3581h	[7:0]	MDSEL13	07h	08h	08h	0Ah	0Ah
3583h	[7:0]	MDSEL14	51h	72h	72h	75h	75h
35B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.				
35B7h	[7:0]						
35B8h	[7:0]	PSSLVS4					
35B9h	[7:0]						
3600h	[7:0]	MDSEL16	0090h	0090h	007Dh	0090h	0090h
3601h	[7:0]						
36BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54.				
36BDh	[7:0]						
3846h	[7:0]	MDSEL9	0000h	0000h	0000h	0000h	0000h
3847h	[7:0]						
384Ah	[7:0]	MDSEL10	0000h	0000h	0000h	0000h	0000h
384Bh	[7:0]						

^{*1} See "Readout Drive Modes" on pages 68 to 69 for details of readout mode No.

^{*2} See "Horizontal/Vertical Operation Period in Each Readout Drive Mode" on page 86 and "Frame Rate Adjustment" on pages 87 for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Description of Register Setting for Each Readout Drive Modes (SLVS-EC)

Address (SLVS-EC)	Bit assign- ment	Register Name	Readout mode No. ^{*1}									
			0	1	1A	7	10					
0003h	[3:0]		0h									
	[6:4]	LANESEL	0h	0h	1h	2h	2h					
	[7]		0h									
0004h	[7:0]	MDSEL1	00h	00h	00h	0Ch	32h					
0005h	[7:0]	MDSEL2	0Bh	06h	06h	41h	35h					
0006h	[7:0]	MDSEL3	02h	02h	02h	02h	02h					
0007h	[7:0]	MDSEL4	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted	A0h: normal / A5h: inverted					
000Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)									
000Fh	[7:0]											
0019h	[0]	MDVREV	0h: vertical direction normal /1h: inverted									
	[7:1]		00h									
002Ch	[7:0]	SHR	According to exposure time (See “Integration Time in Each Readout Drive Mode”)									
002Dh	[7:0]											
0030h	[7:0]	MDSEL5	77h	77h	77h	77h	77h					
0034h	[0]	HOPBOUT_EN	0h	0h	0h	0h	0h					
	[7:1]		00h	00h	00h	00h	00h					
0035h	[0]	HTRIMMING_EN	1h	1h	1h	1h	1h					
	[7:1]		00h	00h	00h	00h	00h					
0036h	[7:0]	HTRIMMING_ START	30h	30h	30h	30h	30h					
0037h	[5:0]											
	[7:6]		0h	0h	0h	0h	0h					
0038h	[7:0]	HTRIMMING_ END	0F00h	0F00h	0F00h	0F00h	0F00h					
0039h	[5:0]											
	[7:6]		0h	0h	0h	0h	0h					
0068h	[7:0]	MDSEL15	0044h	001Ah	001Ah	0044h	0044h					
0069h	[7:0]											
0080h	[7:0]	MDSEL6	00h	00h	01h	00h	00h					
0081h	[7:0]	MDSEL7	01h	01h	01h	01h	01h					
0084h	[7:0]	HCOUNT1	Set XHS period [INCK@72 MHz]									
0085h	[7:0]											
0086h	[7:0]	HCOUNT2	Set XHS period [INCK@72 MHz]									
0087h	[7:0]											
00A8h	[7:0]	MDSEL8	03h	02h	02h	02h	02h					
00E2h	[7:0]	VCUTMODE	00h	00h	00h	04h	07h					
032Ch	[7:0]	PSSLVS1	See “Low Power Consumption Period Length” on page 54.									
032Dh	[7:0]											
034Ah	[7:0]	PSSLVS2										
034Bh	[7:0]											
057Fh	[7:0]	MDSEL11	0Ah	0Ch	0Ch	0Ch	0Ch					
0580h	[7:0]	MDSEL12	09h	0Ah	0Ah	0Ah	0Ah					
0581h	[7:0]	MDSEL13	07h	08h	08h	0Ah	0Ah					
0583h	[7:0]	MDSEL14	51h	72h	72h	75h	75h					
05B6h	[7:0]	PSSLVS3	See “Low Power Consumption Period Length” on page 54.									
05B7h	[7:0]											
05B8h	[7:0]	PSSLVS4										
05B9h	[7:0]											
0600h	[7:0]	MDSEL16	0090h	0090h	007Dh	0090h	0090h					
0601h	[7:0]											
06BCh	[7:0]	PSSLVS0	See “Low Power Consumption Period Length” on page 54.									
06BDh	[7:0]											
0846h	[7:0]	MDSEL9	0000h	0000h	0000h	0000h	0000h					
0847h	[7:0]											
084Ah	[7:0]	MDSEL10	0000h	0000h	0000h	0000h	0000h					
084Bh	[7:0]											

*1 See "Readout Drive Modes" on pages 68 to 69 for details of readout mode No.

Readout Drive Modes (CSI-2 and SLVS-EC)

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.

All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).

1-1. When Using Aspect Ratio Approx. 17:9 (Approx. 9.07 M pixels)

Description of Readout Drive Modes

Readout Mode No.	Readout drive mode	Mode description
1	All-pixel scan mode (AD 12-bit, 12-bit length output)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1A	All-pixel scan mode (AD 12-bit, 12-bit length output) low noise	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1B	All-pixel scan mode horizontal 3840 pixels (AD 12-bit, 12-bit length output) (CSI-2 interface only)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2	All-pixel scan mode (AD 10-bit, 10-bit length output)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2A	All-pixel scan mode (AD 10-bit, 10-bit length output) low noise	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
3	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning) (AD 12-bit, 14-bit length output)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
4	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning) (AD 12-bit, 12-bit length output)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
5	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning) (AD 10-bit, 12-bit length output)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
6	Vertical 2 binning Horizontal 2/4 subsampling (Vertical weighted binning) (AD 10-bit, 10-bit length output)	Add 2 lines with weighting in the vertical direction at the all-pixel scan area and 2 of every 4 lines in the horizontal direction are output. (See the image of binning)
7	Horizontal/vertical 2/4 subsampling (AD 10-bit, 10-bit length output)	2 of every 4 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 2 of every 4 lines in the horizontal direction are output. (See the image of binning)
8	Horizontal/vertical 3/3-line binning (AD 10-bit, 12-bit length output)	Horizontal and vertical direction 3-line binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
9	Vertical 1/3 subsampling horizontal 3 binning (AD 10-bit, 12-bit length output)	1 of every 3 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)
10	Vertical 2/9 subsampling binning horizontal 3 binning (AD 10-bit, 12-bit length output)	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)
11	Vertical 2/9 subsampling binning horizontal 3 binning Low power consumption (AD 10-bit, 10-bit length output)	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)

1-2. When Using Aspect Ratio 4:3 (Approx. 10.71 M pixels)

Description of Readout Drive Modes

Readout Mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (AD 14-bit, 14-bit length output)	All pixels are readout with 14-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (AD 12-bit, 12-bit length output)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1A	All-pixel scan mode (AD 12-bit, 12-bit length output) low noise	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
7	Horizontal/vertical 2/4 subsampling (AD 10-bit, 10-bit length output)	2 of every 4 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 2 of every 4 lines in the horizontal direction are output. (See the image of binning)
10	Vertical 2/9 subsampling binning horizontal 3 binning (AD 10-bit, 12-bit length output)	2 of every 9 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)

2. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.

Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits. So the weight of 1 digit is 4 times greater than during 12-bit output, it will be 16 times larger than that at the time of output of 14-bit output.

Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Vertical pixel processing	Horizontal pixel processing	Total Number of binning pixels	Internal arithmetic processing	Number of output bits
0	14 bits	—	—	—	—	10 bits + 4 bits ^{*1}
1	12 bits	—	—	—	—	10 bits + 2 bits ^{*2}
1A	12 bits	—	—	—	—	10 bits + 2 bits ^{*2}
1B	12 bits	—	—	—	—	10 bits + 2 bits ^{*2}
2	10 bits	—	—	—	—	10 bits
2A	10 bits	—	—	—	—	10 bits
3	12 bits	2 binning	2 binning	4 pixels	$3/6, 1.5/6, 1/6, 0.5/6$ (weighted binning ^{*5})	10 bits + 4 bits ^{*3}
4	12 bits	2 binning	2 binning	4 pixels	$3/6, 1.5/6, 1/6, 0.5/6$ (weighted binning ^{*5})	10 bits + 2 bits ^{*4}
5	10 bits	2 binning	2 binning	4 pixels	$3/6, 1.5/6, 1/6, 0.5/6$ (weighted binning ^{*5})	10 bits + 2 bits ^{*4}
6	10 bits	2 binning	2/4 subsampling	2 pixels	$3/4, 1/4$ (weighted binning ^{*5})	10 bits
7	10 bits	2/4 subsampling	2/4 subsampling	—	—	10 bits
8	10 bits	3 binning	3 binning	9 pixels	1/9	10 bits + 2 bits ^{*4}
9	10 bits	1/3 subsampling	3 binning	3 pixels	1/3	10 bits + 2 bits ^{*4}
10	10 bits	2/9 subsampling binning	3 binning	6 pixels	1/6	10 bits + 2 bits ^{*4}
11	10 bits	2/9 subsampling binning	3 binning	6 pixels	1/6	10 bits

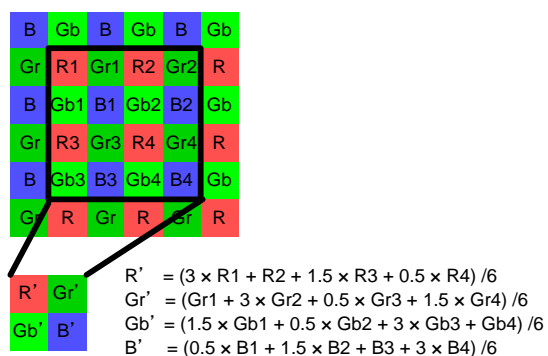
^{*1} A/D conversion is performed with a resolution 16 times that of 10-bit A/D conversion, and the results are output in 14 bits regarded as a 10-bit integer item and a 4-bit decimal item.

^{*2} A/D conversion is performed with a resolution 4 times that of 10-bit A/D conversion, and the results are output in 12 bits regarded as a 10-bit integer item and a 2-bit decimal item.

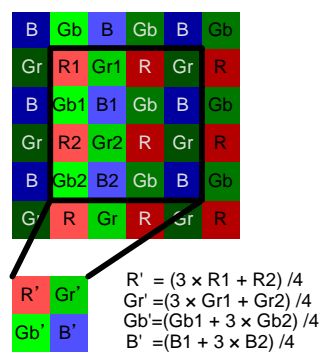
^{*3} Division is performed by internal arithmetic processing, then the results are output in 14 bits with the integer item in the upper 10 bits and the decimal item in the lower 4 bits.

^{*4} Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.

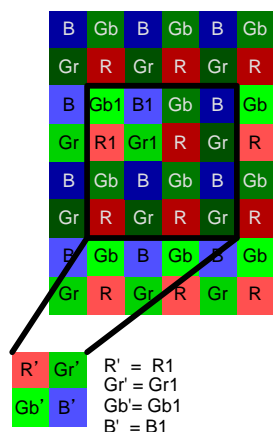
^{*5} See "Binning Image" for details of weighted binning in the following figures.



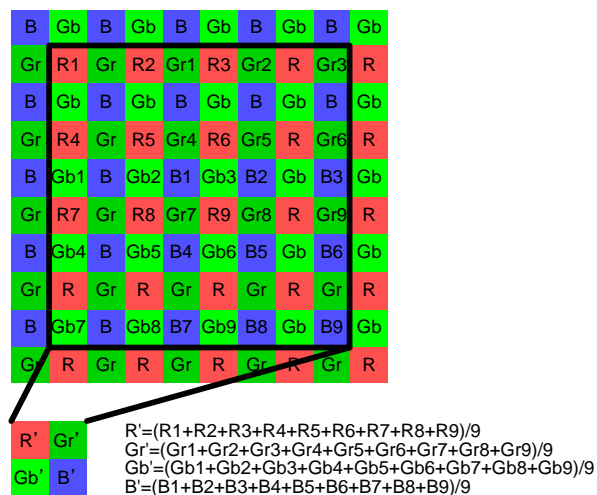
Horizontal/Vertical 2/2-line Binning
(Horizontal and vertical weighted binning)
Binning Image



Vertical 2 Binning Horizontal 2/4 Subsampling
(Vertical weighted binning)
Binning Image



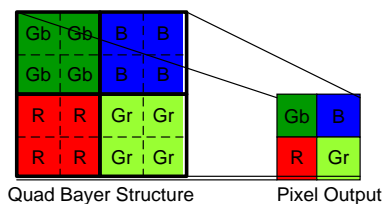
Horizontal/Vertical 2/4 Subsampling
Binning Image

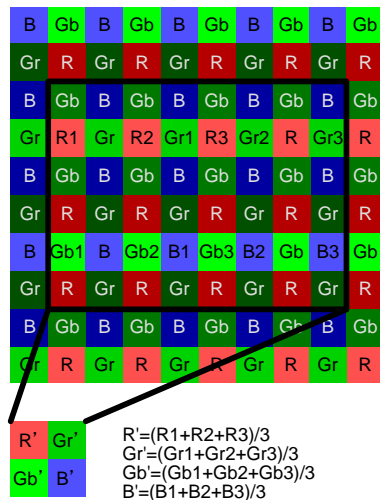


Horizontal/Vertical 3/3-line Binning
Binning Image

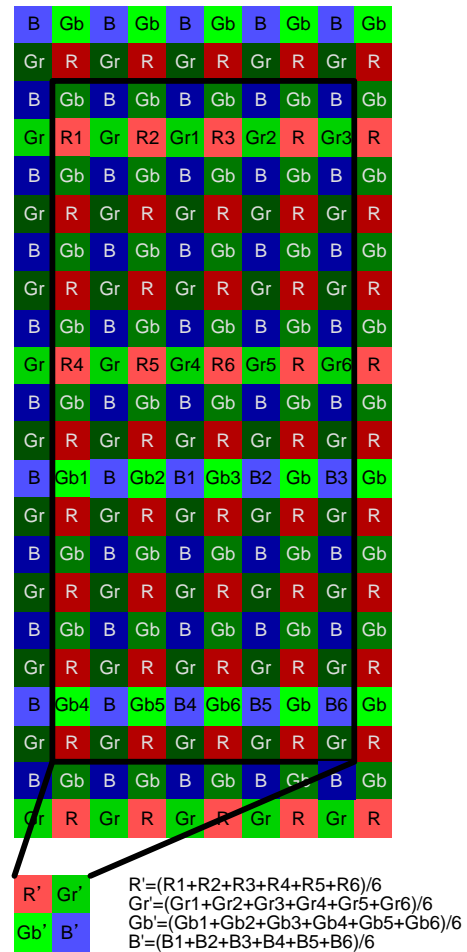
Note) White letters in the diagram indicate pixels which are not read out.

Bayer 1 pixel in the figure is made up of the same color four pixels of Quad Bayer structure.





Vertical 1/3 Subsampling Binning
Horizontal 3 Binning
Binning Image



Vertical 2/9 Subsampling Binning
Horizontal 3 Binning
Binning Image

Note) White letters in the diagram indicate pixels which are not read out.

Bayer 1 pixel in the figure is made up of the same color four pixels of Quad Bayer structure.

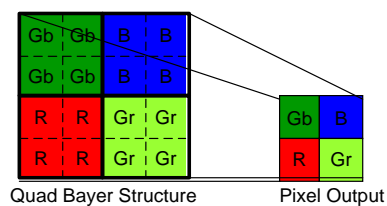


Image Data Output Format When Using CSI-2

Frame Format (CSI-2)

Each line of each image frame is output like the General Frame Format to CSI-2.
The settings for each packet header are shown below.

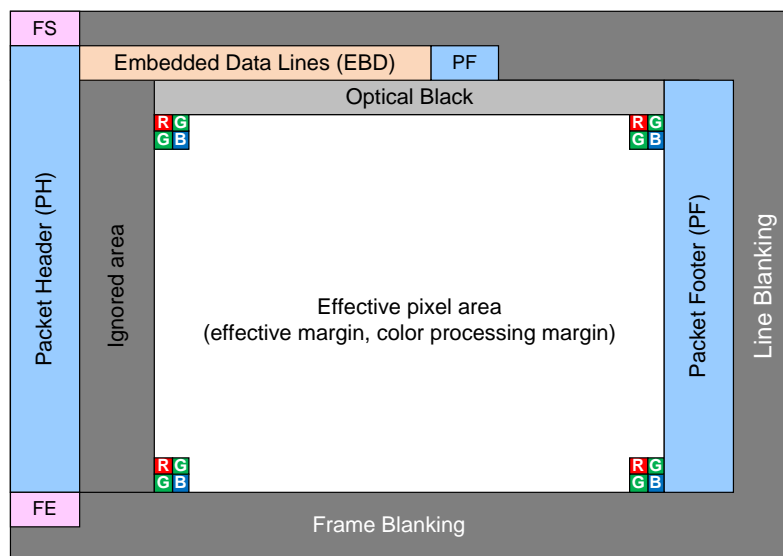
DATA Type

Header [5:0]	Name	Description
00h	Frame Start Code	FS
01h	Frame End Code	FE
12h	Embedded Data	Embedded data
2Bh ^{*1}	RAW10	When output data bit length is 10-bits
2Ch ^{*1}	RAW12	When output data bit length is 12-bits
2Dh ^{*1}	RAW14	When output data bit length is 14-bits
37h ^{*1}	Optical Black Data	Vertical Optical Black line data

^{*1} When using the HDR function, data type will change in the long-term integration frame and the short-time integration frame. See the document "IMX294 Application Note Quad Bayer Coding HDR" for details.

Frame Structure (CSI-2)

The figure below shows the image frame structure.
The Embedded data line is output in the 1 lines following the sync code FS.

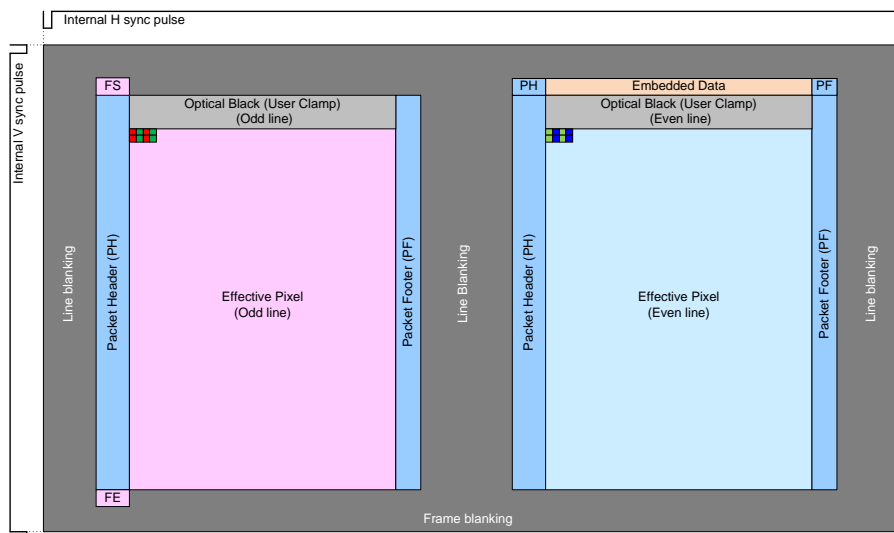


Frame Structure (CSI-2)

Data Output Format (CSI-2)

The figure below shows the data output format.

Output data of the two lines per 1 internal horizontal sync pulse.



Data Output Format (CSI-2)

Embedded Data Line (CSI-2)

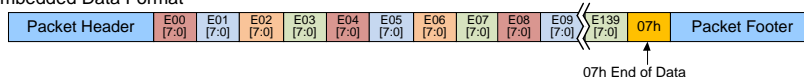
The Embedded data line is output in a line following the sync code FS.

In RAW10 mode, 55h dummy bytes are inserted after outputting 4 bytes of data each.

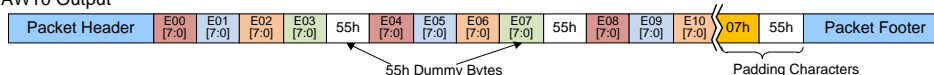
In RAW12 mode, 55h dummy bytes are inserted after outputting 2 bytes of data each.

In RAW14 mode, 55h dummy bytes are inserted after outputting 4 bytes of data each.

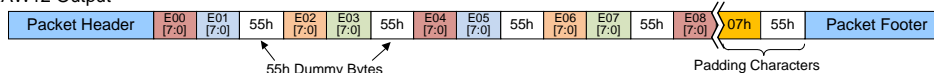
Embedded Data Format



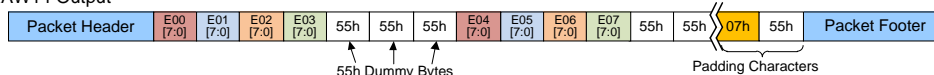
RAW10 Output



RAW12 Output



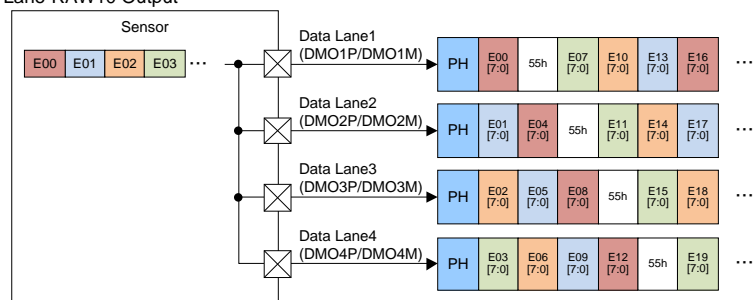
RAW14 Output



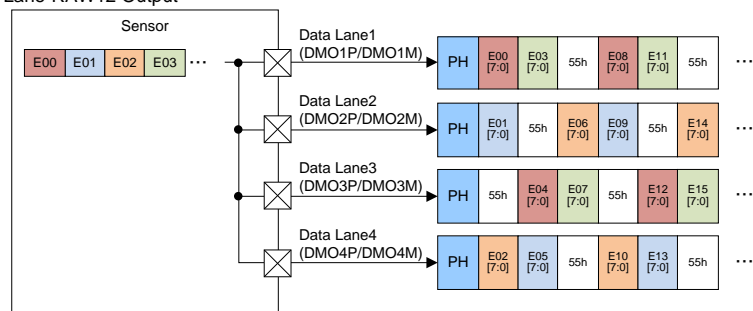
Embedded Data Line Format (CSI-2)

The each format of 4 Lane is shown below.

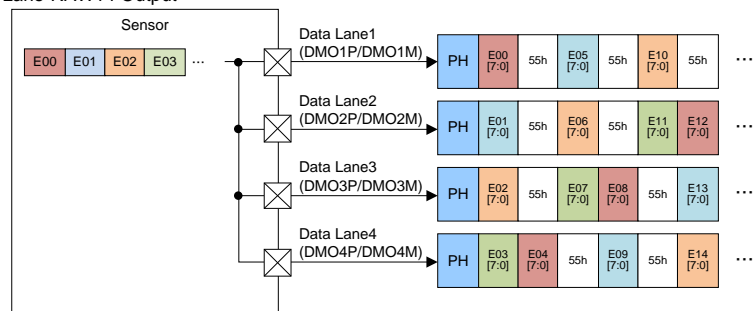
a) 4 Lane-RAW10 Output



b) 4 Lane-RAW12 Output



c) 4 Lane-RAW14 Output



Output Format of Embedded 4 Lane (CSI-2)

Specific Output (CSI-2)

Output timing	bit	Transfer data	Description
E00 to E05	[7:0]	—	(Ignored)
E06	[0]	SMD	
	[7:1]	—	(Ignored)
E07	[7:0]	PGC	
E08	[2:0]		
	[7:3]	—	(Ignored)
E09	[7:0]	SHR	
E10	[7:0]		
E11	[7:0]	SVR	
E12	[7:0]		
E13 to E14	[7:0]	—	(Ignored)
E15	[3:0]	DGAIN	
	[4]	MDVREV	
	[7:5]	—	(Ignored)
E16 to E20	[7:0]	—	(Ignored)
E21	[7:0]	BLKLEVEL	
E22	[1:0]		
	[7:2]	—	(Ignored)
E17 to E24	[7:0]	—	(Ignored)
E25	[0]	HTRIMMING_EN	
	[7:1]	—	(Ignored)
E26	[7:0]	HTRIMMING_START	
E27	[5:0]		
	[7:6]	—	(Ignored)
E28	[7:0]	HTRIMMING_END	
E29	[5:0]		
	[7:6]	—	(Ignored)
E30	[0]	VWIDCUTEN	
	[3:1]	—	(Ignored)
	[7:4]	—	(Ignored)
E31	[7:0]	VWINPOS	
E32	[5:0]		
	[7:6]	—	(Ignored)
E33	[7:0]	VWIDCUT	
E34	[5:0]		
	[7:6]	—	(Ignored)
E35 to E143	[7:0]	—	(Ignored)

CSI-2 serial Output Setting (CSI-2)

The output formats of this sensor support the following modes.

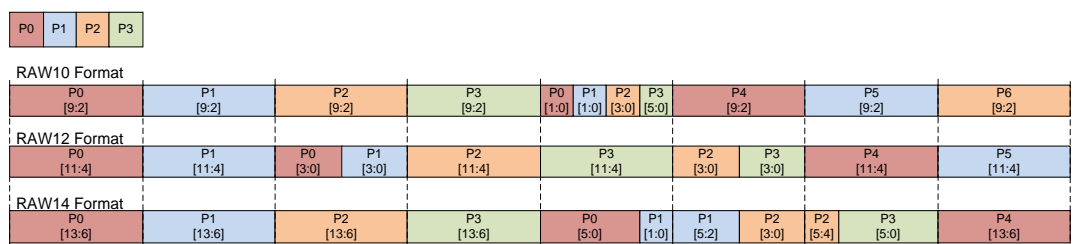
CSI-2 serial data output 4 Lane, RAW10, RAW12 and RAW14

The image data is output from the CSI-2 output pin. The DMO1P/DMO1M are called the Lane1 data signal, the DMO2P/DMO2M are called the Lane2 data signal, the DMO3P/DMO3M are called the Lane3 data signal and the DMO4P/DMO4M are called the Lane4 data signal. In addition, the clock signals are output from DCKP/DCKM of the CSI-2 pins.

In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.

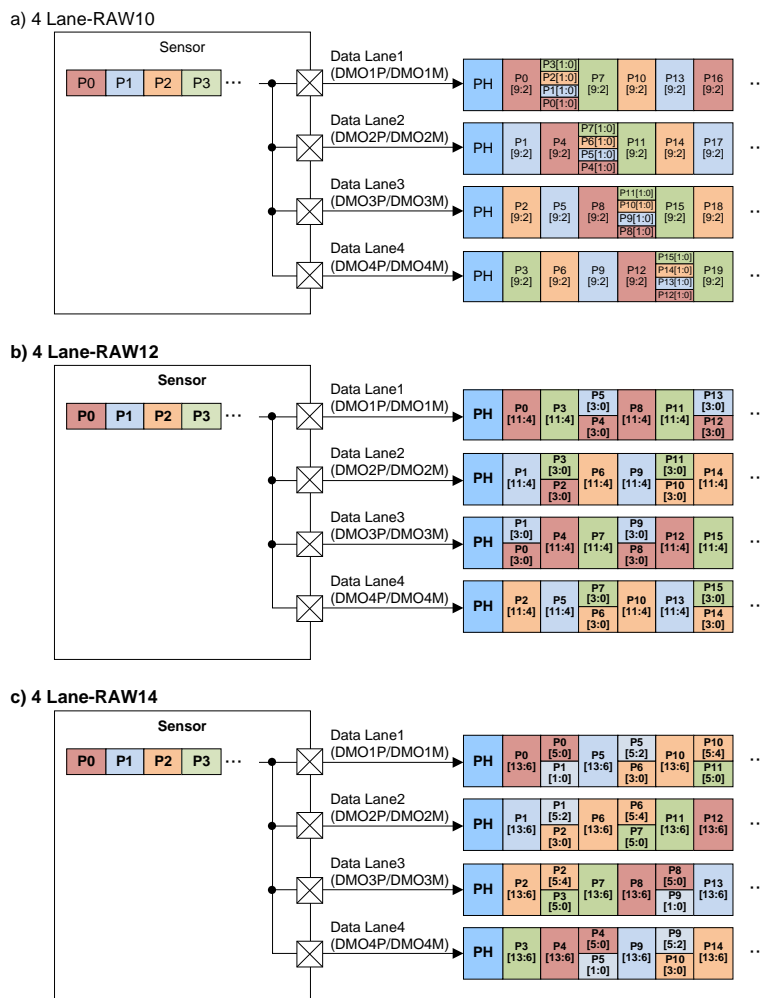
The bit rate maximum value is 1.728 Gbps/Lane.

The formats of RAW10 and RAW12 are shown below.



Example of formats of RAW10, RAW12 and Raw14

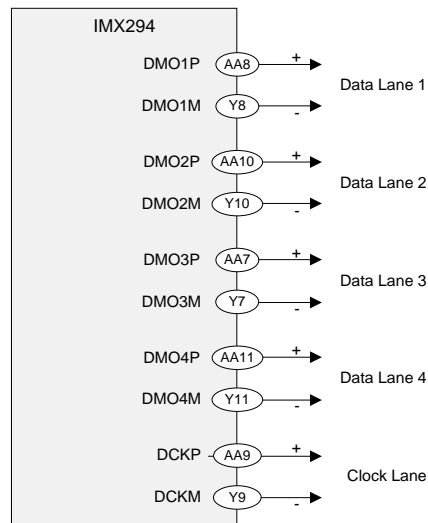
The each format of 4 Lane are shown below.



Output Format of 4 Lane (CSI-2)

MIPI Transmitter (CSI-2)

Output pins (DMO1P to DMO4P, DMO1M to DMO4M, DCKP, DCKM) are described in this section.



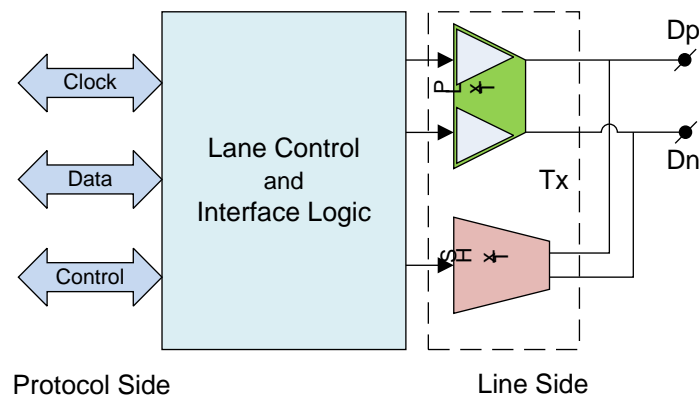
Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.

See the MIPI Standard

- MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1.728Gbps/Lane.



Universal Lane Module Functions

Detailed Specification of Each Mode (CSI-2)

1. When Using Aspect Ratio Approx. 17:9 (Approx. 9.07 M pixels)

1-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Horizontal Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX register minimum value	HMAX number per H period
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel		
1	0	24	12	4096	12	0	1122	0.5
1A	0	24	12	4096	12	32	1192	0.5
1B	0	8	12	3840	12	0	1055	0.5
2	0	24	12	4096	12	0	947	0.5
2A	0	24	12	4096	12	32	954	0.5
3	0	12	6	2048	6	16	706	1
4	0	12	6	2048	6	16	706	1
5	0	12	6	2048	6	16	607	1
6	0	12	6	2048	6	16	520	1
7	0	12	6	2048	6	16	520	0.5
8	0	8	4	1364	4	12	520	1.5
9	0	8	4	1364	4	12	520	0.5
10	0	8	4	1364	4	12	520	1
11	0	8	4	1364	4	12	520	4

Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX register minimum value
	Front OB	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
1	8	8	4	2160	4	0	1111
1A	8	8	4	2160	4	0	1111
1B	8	8	4	2160	4	0	1111
2	8	8	4	2160	4	0	1116
2A	8	8	4	2160	4	0	1116
3	4	4	6	1080	6	0	1148
4	4	4	6	1080	6	0	1148
5	4	4	6	1080	6	0	1148
6	4	4	6	1080	6	0	1148
7	4	4	6	1080	6	0	574
8	4	4	6	720	6	0	1182
9	4	4	6	720	6	0	394
10	4	4	2	240	2	0	300
11	4	2	2	240	2	0	298

1-2. Frame Rate Adjustment (CSI-2)

The formula for frame rate calculation is shown below.

$$\text{Frame rate [frame/s]} = (72 \times 10^6) / \{ \text{HMAX register value} \times \text{VMAX register value} \times (\text{SVR register value} + 1) \}$$

The frame rate can be changed by changing HMAX and VMAX register values as long as these are set to minimum value or larger. HMAX changes the line blanking period. VMAX changes the frame blanking period.

The examples of setting for each readout drive mode are shown in the table below. Set HMAX and VMAX considering ISP image processing time.

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See "Electronic Shutter Timing" for details.

Examples of HMAX, VMAX and Frame Rate (CSI-2)

Readout mode No.	HMAX ^{*1} min value	VMAX ^{*2} min value	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				HMAX ^{*1} [dec]	VMAX ^{*2} [dec]	SVR	Frame frequency [frame/s]	HMAX ^{*1} [dec]	VMAX ^{*2} [dec]	SVR	Frame frequency [frame/s]
1	1122	1111	57.76	1200	1250	0	48.00 ^{*3}	1152	1250	0	50.00
1A	1192	1111	54.37	1200	2002	0	29.97	1250	2304	0	25.00
1B	1055	1111	61.43	1200	1250	0	48.00 ^{*3}	1125	1280	0	50.00
2	947	1116	68.13	975	1232	0	59.94	1000	1440	0	50.00
2A	954	1116	67.63	975	1232	0	59.94	1000	1440	0	50.00
3	706	1148	88.84	715	1680	0	59.94	720	2000	0	50.00
4	706	1148	88.84	715	1680	0	59.94	720	2000	0	50.00
5	607	1148	103.32	616	1950	0	59.94	625	2304	0	50.00
6	520	1148	120.61	520	1155	0	119.88	576	1250	0	100.00
7	520	574	241.22	520	1155	0	119.88	576	1250	0	100.00
7 (60fps)				520	1155	1	59.94	576	1250	1	50.00
8	520	1182	117.14	520	2310	0	59.94	720	2000	0	50.00
8 (30fps)				520	2310	1	29.97	720	2000	1	25.00
9	520	394	351.43	520	462	0	299.70	576	500	0	250.00
9 (60fps)				520	462	4	59.94	576	500	4	50.00
10	520	300	461.54	520	462	0	299.70	576	500	0	250.00
10 (60fps)				520	462	4	59.94	576	500	4	50.00
11	520	298	58.08 ^{*4}	525	572	7	29.97	576	625	7	25.00

^{*1} The value set as HMAX (address 30ACh, bit [7:0] and address 30ADh, bit [7:0]).

^{*2} The value set as VMAX (address 30A9h, bit [7:0], address 30AAh, bit [7:0] and address 30ABh, bit [3:0]).

^{*3} The frame rate is not compatible for NTSC.

^{*4} Low power consumption drive (SVR = 7h)

1-3. Imaging Conditions in Each Readout Drive Mode (CSI-2)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
1	4	12	RAW12	4096	2160	Approximately 8.85 M Pixels
1A	4	12	RAW12	4096	2160	Approximately 8.85 M Pixels
1B	4	12	RAW12	3840	2160	Approximately 8.29 M Pixels
2	4	10	RAW10	4096	2160	Approximately 8.85 M Pixels
2A	4	10	RAW10	4096	2160	Approximately 8.85 M Pixels
3	4	12	RAW14	2048	1080	Approximately 2.21 M Pixels
4	4	12	RAW12	2048	1080	Approximately 2.21 M Pixels
5	4	10	RAW12	2048	1080	Approximately 2.21 M pixels
6	4	10	RAW10	2048	1080	Approximately 2.21 M pixels
7	4	10	RAW10	2048	1080	Approximately 2.21 M pixels
8	4	10	RAW12	1364	720	Approximately 0.98 M pixels
9	4	10	RAW12	1364	720	Approximately 0.98 M pixels
10	4	10	RAW12	1364	240	Approximately 0.33 M pixels
11	4	10	RAW10	1364	240	Approximately 0.33 M pixels

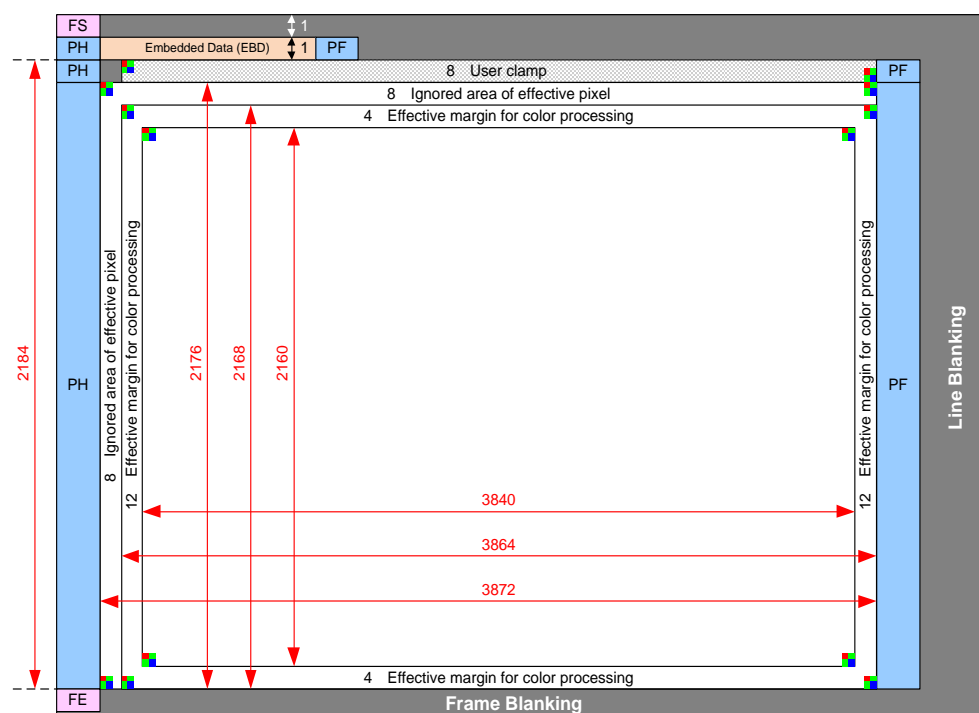
(CSI-2) MODE1: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)
(CSI-2) MODE2: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)



(CSI-2) MODE2A: All-pixel scan mode low noise
(10-bit A/D conversion, 10-bit length output)



(CSI-2) MODE1B: All-pixel scan mode horizontal 3840 pixels (12-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (3840 × 2160)

(CSI-2) MODE3: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)

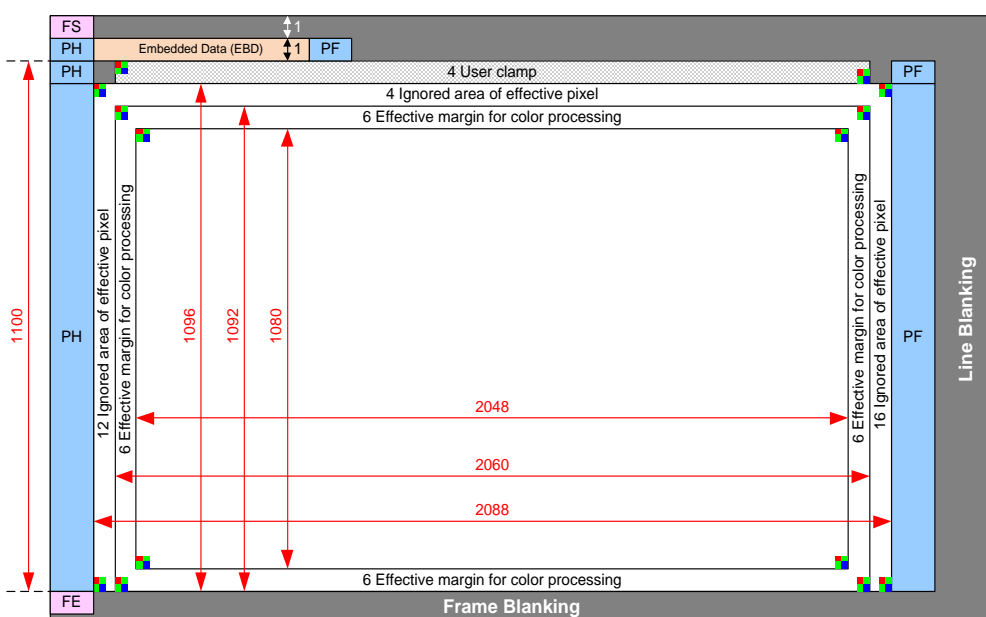
(12-bit A/D conversion, 14-bit length output)

(CSI-2) MODE4: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)

(12-bit A/D conversion, 12-bit length output)

(CSI-2) MODE5: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)

(10-bit A/D conversion, 12-bit length output)



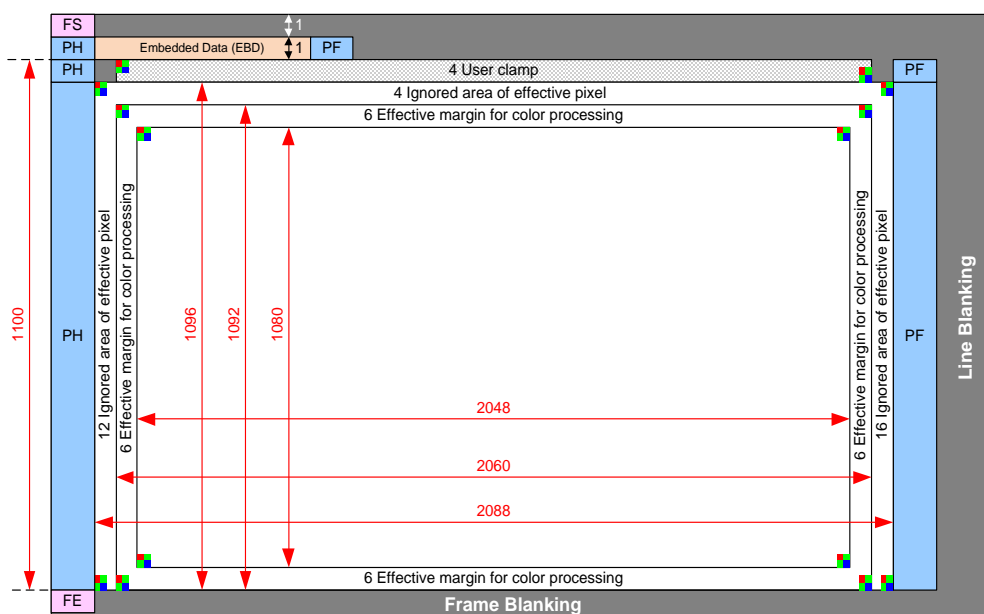
Readout Pixel Image Diagram (2048 × 1080)

(CSI-2) MODE6: Vertical 2 binning horizontal 2/4 subsampling (vertical weighted binning)

(10-bit A/D conversion, 10-bit length output)

(CSI-2) MODE7: Horizontal/vertical 2/4 subsampling

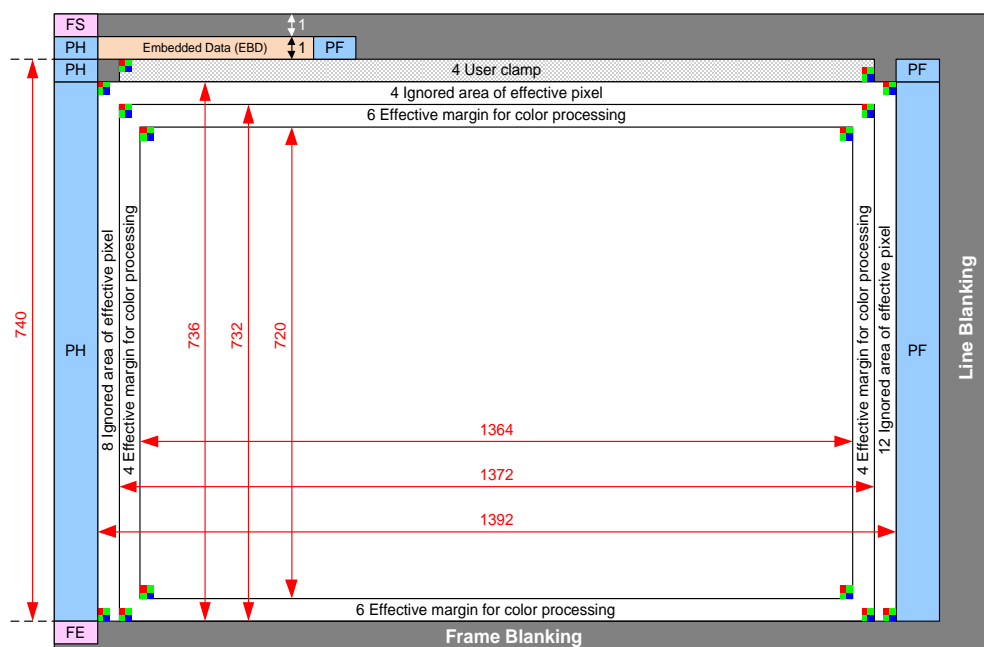
(10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (2048 × 1080)

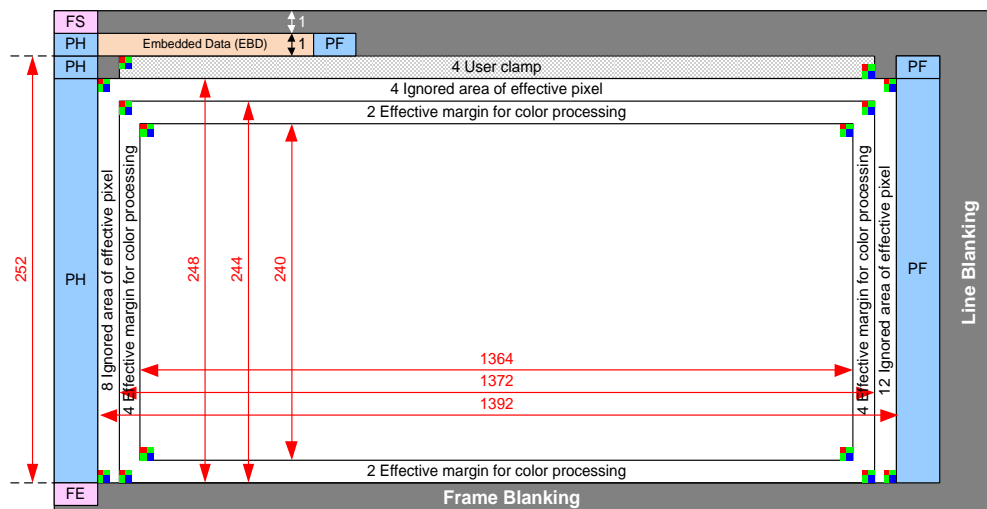
(CSI-2) MODE8: Horizontal/vertical 3/3-line binning (10-bit A/D conversion, 12-bit length output)

(CSI-2) MODE9: Vertical 1/3 subsampling horizontal 3 binning (10-bit A/D conversion, 12-bit length output)



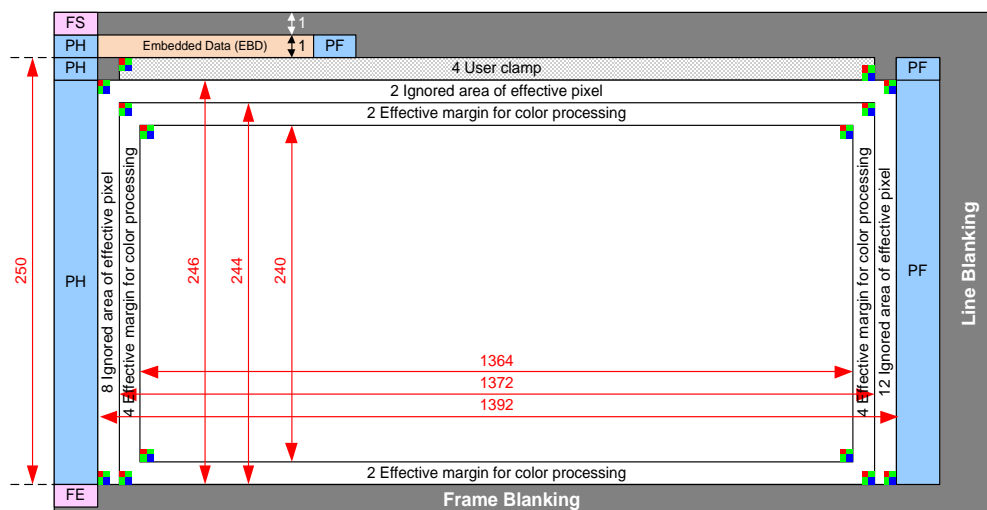
Readout Pixel Image Diagram (1364 × 720)

**(CSI-2) MODE10: Vertical 2/9 subsampling binning horizontal 3 binning
(10-bit A/D conversion, 12-bit length output)**



Readout Pixel Image Diagram (1364 × 240)

**(CSI-2) MODE11: Vertical 2/9 subsampling binning horizontal 3 binning low power consumption drive
(10-bit A/D conversion, 10-bit length output)**



Readout Pixel Image Diagram (1364 × 240)

2. When Using Aspect Ratio 4:3 (Approx. 10.71 M pixels)

2-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Horizontal Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX register minimum value	HMAX number per H period
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel		
0	0	28	12	3704	12	36	1730	0.5
1	0	28	12	3704	12	36	1034	0.5
1A	0	28	12	3704	12	36	1192	0.5
7	0	14	6	1852	6	18	520	0.5
10	0	10	4	1234	4	12	520	1

Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						VMAX register minimum value
	Front OB	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	16	8	18	2778	18	2	1444
1	16	8	18	2778	18	2	1444
1A	16	8	18	2778	18	2	1444
7	4	4	6	1388	6	0	728
10	4	4	2	308	2	0	368

2-2. Frame Rate Adjustment (CSI-2)

The formula for frame rate calculation is shown below.

$$\text{Frame rate [frame/s]} = (72 \times 10^6) / \{ \text{HMAX register value} \times \text{VMAX register value} \times (\text{SVR register value} + 1) \}$$

The frame rate can be changed by changing HMAX and VMAX register values as long as these are set to minimum value or larger. HMAX changes the line blanking period. VMAX changes the frame blanking period.

The examples of setting for each readout drive mode are shown in the table below. Set HMAX and VMAX considering ISP image processing time.

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register.

When using SVR = 1h, the frame rate becomes half. See "Electronic Shutter Timing" for details.

Examples of HMAX, VMAX and Frame Rate (CSI-2)

Readout mode No.	HMAX ^{*1} min value	VMAX ^{*2} min value	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				HMAX ^{*1} [dec]	VMAX ^{*2} [dec]	SVR	Frame frequency [frame/s]	HMAX ^{*1} [dec]	VMAX ^{*2} [dec]	SVR	Frame frequency [frame/s]
0	1730	1444	28.82	1875	1600	0	24.00 ^{*3}	1800	1600	0	25.00
1	1034	1444	48.22	1040	2310	0	29.97	1125	2560	0	50.00
1A	1192	1444	41.83	1232	1950	0	29.97	1250	2304	0	50.00
7	520	728	190.19	525	1144	0	119.88	576	1250	0	100.00
7(60fps)				525	1144	1	59.94	576	1250	1	50.00
10	520	368	376.25	520	385	0	359.64	600	400	0	300.00
10(30fps)				520	385	11	29.97	600	400	11	25.00

^{*1} The value set as HMAX (address 30ACh, bit [7:0] and address 30ADh, bit [7:0]).

^{*2} The value set as VMAX (address 30A9h, bit [7:0], address 30AAh, bit [7:0] and address 30ABh, bit [3:0]).

^{*3} The frame rate is not compatible for NTSC.

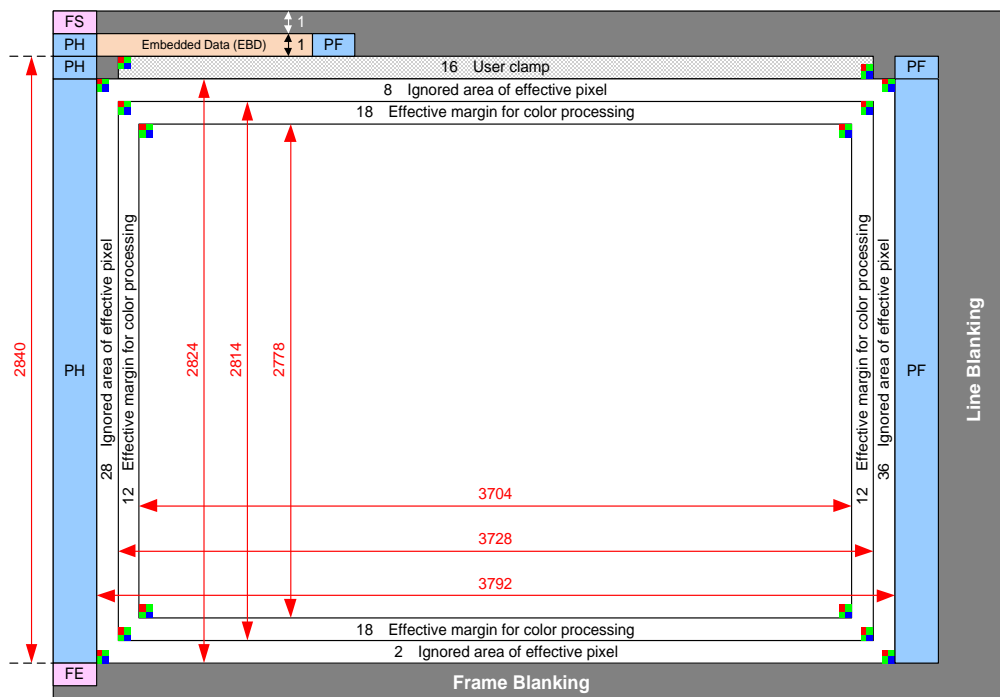
2-3. Imaging Conditions in Each Readout Drive Mode (CSI-2)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	4	14	RAW14	3704	2778	Approximately 10.29 M Pixels
1	4	12	RAW12	3704	2778	Approximately 10.29 M Pixels
1A	4	12	RAW12	3704	2778	Approximately 10.29 M Pixels
7	4	10	RAW10	1852	1388	Approximately 2.57 M Pixels
10	4	10	RAW12	1234	308	Approximately 0.38 M Pixels

2-4. Image Data Output Format (CSI-2)

(CSI-2) MODE0: All-pixel scan mode (14-bit A/D conversion, 14-bit length output)

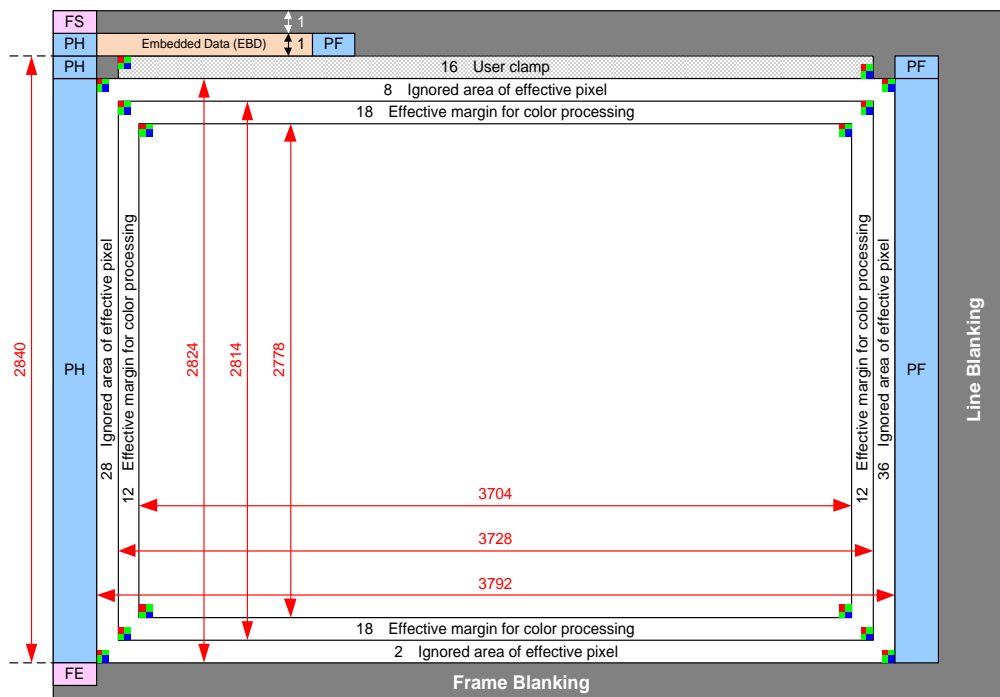
(CSI-2) MODE1: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (3704 x 2778)

(CSI-2) MODE1A: All-pixel scan mode low noise

(12-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (3704 x 2778)

[illegible][illegible]

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Vertical Arbitrary Cropping Function (CSI-2)

Vertical cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings (CSI-2)

Enable vertical cropping with setting vertical arbitrary cropping enable register VWIDCUTEN to 1h, and specify cropping width by the vertical cropping width register VWIDCUT, and cropping position by the vertical cropping start position register VWINPOS.

And set the number of total output lines (including VOB) after cropping to the register WRITE_VSIZE, and the number of effective pixel lines (not including VOB) after cropping to the register Y_OUT_SIZE.

Set VWINPOS negative value (two's complement) when the direction of vertical readout is inverted (MDVREV = 1h).

V_{eff} indicates the number of effective lines output before cropping (VWIDCUTEN = 0h) in following description.

VWIDCUTEN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
VWIDCUTEN	30DDh	—	[0]	0h	Vertical arbitrary cropping is disabled
				1h	Vertical arbitrary cropping is enabled

VWIDCUT Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
VWIDCUT [7:0]	30DEh	—	[7:0]	Specify vertical cropping width
VWIDCUT [13:8]	30DFh	—	[5:0]	Output height [line] = $V_{eff} - VWIDCUT \times \text{step}$

VWINPOS Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
VWINPOS [7:0]	30E0h	—	[7:0]	Vertical cropping start position (two's complement)
VWINPOS [13:8]	30E1h	—	[5:0]	New start position (in output image) [line] = $VWINPOS \times \text{step}$

WRITE_V_SIZE Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
WRITE_VSIZE [7:0]	3130h	—	[7:0]	Set the number of total output lines (including VOB) after cropping
WRITE_VSIZE [12:8]	3131h	—	[4:0]	

Y_OUT_SIZE Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
Y_OUT_SIZE [7:0]	3132h	—	[7:0]	Set the number of effective pixel lines (not including VOB) after cropping
Y_OUT_SIZE [12:8]	3133h	—	[4:0]	

Refer to the following table in the value of step.

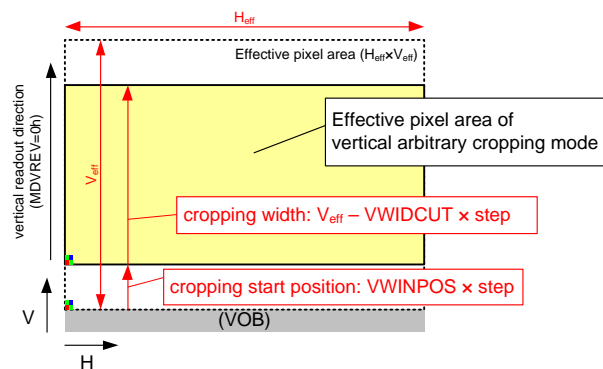
Vertical Arbitrary Cropping Step

Readout mode No.	step value
4, 6, 11	2
0, 1, 1A, 1B, 2, 2A, 3, 5, 7, 8, 9, 10	4

When vertical readout direction is normal (MDVREV = 0h), relation between register setting values of VWINPOS / VWIDCUT and cropping region on physical pixel array is shown below.

Register setting values must satisfy following relations. (Setting ranges are within those values which satisfy following.)

- $V_{\text{WINPOS}} \times \text{step} \geq 0$ (Starting position of readout must be 0 or more)
- $V_{\text{eff}} - V_{\text{WIDCUT}} \times \text{step} \geq V_{\text{eff}} / 2$ (Number of readout lines must be 1/2 or more before cropping)
- $V_{\text{WINPOS}} \times \text{step} + V_{\text{eff}} - V_{\text{WIDCUT}} \times \text{step} \leq V_{\text{eff}}$ (End position of readout must be within the area before cropping)

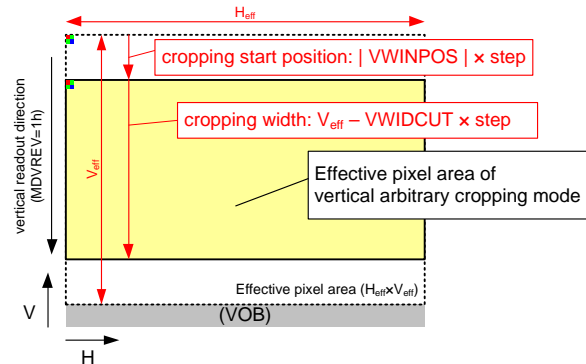


Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array (Vertical Readout Direction Normal)

For example, when the top 400 lines and bottom 400 lines (totally 800 lines) of aspect ratio approx. 17:9 mode1 all-pixel scan area is skipped and start cropping readout from the 401st line, setting values are as follows:
VWIDCUT 00C8h (200d) / VWINPOS 0064h (100d) / WRITE_VSIZE 0568h (1384d) / Y_OUT_SIZE 0560h (1376d)
(step = 4 for mode1)

When vertical readout direction is inverted (MDVREV = 1h), relation between register setting value of VWINPOS / VWIDCUT and cropping region is shown below. Register setting values must satisfy following relations also. Note that VWINPOS must be negative.

$|VWINPOS| \times \text{step} \geq 0$ (Starting position of readout must be 0 or more)
 $V_{\text{eff}} - VWIDCUT \times \text{step} \geq V_{\text{eff}} / 2$ (Number of readout lines must be 1/2 or more before cropping)
 $|VWINPOS| \times \text{step} + V_{\text{eff}} - VWIDCUT \times \text{step} \leq V_{\text{eff}}$ (End position of readout must be within the area before cropping)



Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array (Vertical Readout Direction Inverted)

For example, when the top 400 lines and bottom 400 lines (total 800 lines) of aspect ratio approx. 17:9 mode1 all-pixel scan area (when vertical readout direction inverted) is skipped and start cropping readout from the 401st line, setting values are as follows:
 VWIDCUT 00C8h (200d) / VWINPOS FF9Ch (-100d) / WRITE_VSIZE 0568h (1384d) / Y_OUT_SIZE 0560h (1376d) (step = 4 for mode1)

(2) Vertical Minimum Period When Using Vertical Arbitrary Cropping Function (CSI-2)

When using vertical arbitrary cropping function, VMAX minimum value gets smaller according to cropping width. VMAX minimum value after cropping follows the formula below using V_{MAX0} (VMAX minimum value before cropping).

$$V_{\text{MAX}} \text{ minimum value} = V_{\text{MAX0}} - VWIDCUT \times \text{step} \times H_{\text{MAX}} \text{ number per H period}$$

For example, when using readout mode No.1 of aspect ratio approx. 17:9 mode1 all-pixel scan area (approx. 9.07M pixels), if you use cropping of VWIDCUT=00C8h(=200d), VMAX minimum value is $1111 - 200 \times 4 \times 0.5 = 711$. ($V_{\text{MAX0}} = 1111$ and HMAX number per H period is 0.5)

Horizontal Arbitrary Cropping Function (CSI-2)

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings (CSI-2)

Set horizontal cropping enable register HTRIMMING_EN to 1h to enable horizontal arbitrary cropping function, and horizontal cropping area are determined by horizontal cropping position register HTRIMMING_START and HTRIMMING_END.

HTRIMMING_EN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function	Remarks
HTRIMMING_EN	3035h	—	[0]	0h	Horizontal arbitrary cropping OFF	Send with register setting for each readout drive mode.
				1h	Horizontal arbitrary cropping ON	

Horizontal Arbitrary Cropping Position Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Remarks
HTRIMMING_START [7:0]	3036h	—	[7:0]	horizontal cropping start position [†]	Unit: pixel Send with register setting for each readout drive mode.
HTRIMMING_START [13:8]	3037h	—	[5:0]		
HTRIMMING_END [7:0]	3038h	—	[7:0]	horizontal cropping end position [†] + 1	
HTRIMMING_END [13:8]	3039h	—	[5:0]		

^{*1} In the readout mode with horizontal binning or subsampling, set the value of HTRIMMING_START and HTRIMMING_END according to the position before processing horizontal binning or subsampling.

HTRIMMING_START and HTRIMMING_END must satisfy following 3 restrictions.

$$\begin{aligned} \text{HTRIMMING_START} &= 48 + N \times \text{step1} \\ \text{HTRIMMING_END} &= \text{HNUM} - M \times \text{step2} \\ \text{HTRIMMING_END} - \text{HTRIMMING_START} &\geq \text{Minimum value.} \\ (\text{M and N are integers equal or more than 0}) \end{aligned}$$

Refer to the following tables in the value of step1, step2, HNUM and Minimum value.

Step value

Readout mode Horizontal pixel processing	no binning	Horizontal 2 binning	Horizontal 3 binning	Horizontal 2/4 subsampling
step1	12	12	12	24
step2	4	24	12	24

Minimum value of HTRIMMING_END – HTRIMMING_START

Readout mode Horizontal pixel processing	no binning	Horizontal 2 binning	Horizontal 3 binning	Horizontal 2/4 subsampling
Minimum value	36	72	96	72

HNUM value

Readout mode No.	When Using Aspect Ratio Approx. 17:9 (Approx. 9.07M pixels)			When Using Aspect Ratio 3:2 (Approx. 10.71M pixels)
	1, 2	1B	1A, 2A, 3, 4, 5, 6, 7, 8, 9, 10, 11	0, 1, 1A, 7, 10
HNUM	4192	3920	4224	3840

(2) Horizontal Minimum Period When Using Horizontal Arbitrary Cropping Function (CSI-2)

When using horizontal arbitrary cropping function, HMAX minimum value is as follows:

HMAX Minimum Value When Using Horizontal Arbitrary Cropping Function

Readout mode No.	HMAX minimum value
0	1730
1	$\max(706, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 1/4 + 85.3)$
1A	1192
1B	$\max(706, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 1/4 + 85.3)$
2	$\max(520, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 5/24 + 83.2)$
2A	$\max(827, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 5/24 + 83.2)$
3	706
4	706
5	$\max(520, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 1/8 + 85.3)$
6	520
7	520
8	520
9	520
10	520
11	520

* $\max(A, B)$ means the larger value of A and B.

* Fractions should be rounded up.

Electronic Shutter Timing When Using CSI-2

1. SHR, SVR, SMD Setting When Using CSI-2

1-1. SHR, SVR Setting (CSI-2)

The exposure start timing can be designated by setting the electronic shutter timing register SHR. Note that this setting value unit is $1[\text{HMAX}]^{*1}$ period regardless of the readout drive mode.

In addition, 1 frame period can be extended at VMAX period unit according to the SVR register.

(1 frame cycle is (SVR value + 1) times as long as VMAX period.)

^{*1} Setting value of register HMAX × 72MHz clock

Shutter Control Register (CSI-2)

Name	CSI-2 (I ² C) Address	Bit	Function
SHR [7:0]	302Ch	[7:0]	Specifies the integration start horizontal period
SHR [15:8]	302Dh	[7:0]	
SVR [7:0]	300Eh	[7:0]	Specifies the integration shutdown vertical period
SVR [15:8]	300Fh	[7:0]	
HMAX [7:0]	30ACh	[7:0]	Horizontal drive period length
HMAX [15:8]	30ADh	[7:0]	
VMAX [7:0]	30A9h	[7:0]	Vertical drive period length
VMAX [15:8]	30AAh	[7:0]	
VMAX [19:16]	30ABh	[3:0]	

Shutter Control Register Setting Range (CSI-2)

Register	Register Value		Function
SHR	5 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No.0, 1, 1A, 1B, 2, 2A All-pixel scan mode (14 bits, 12 bits, 10 bits) All-pixel scan mode (12 bits) low noise All-pixel scan mode (10 bits) low noise	Specifies the integration start horizontal period
	5 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No.3, 5 Horizontal/vertical 2/2-line binning mode (Horizontal and vertical weighted binning)	
	3 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No.4 Horizontal/vertical 2/2-line binning mode (Horizontal and vertical weighted binning)	
	5 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No. 6 Vertical 2 binning horizontal 2/4 subsampling (Vertical weighted binning)	
	3 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No. 7 Horizontal/vertical 2/4 subsampling	
	7 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No.8, Horizontal/vertical 3/3 binning	
	2 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No.9 Vertical 1/3 subsampling Horizontal 3 binning	
	5 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 1\}$	Readout mode No. 10 Vertical 2/9 subsampling binning Horizontal 3 binning	
	5 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} / 4 - 1\}$	Readout mode No. 11 Vertical 2/9 subsampling binning Horizontal 3 binning, low power consumption	
	1 to $\{(SVR \text{ value} + 1) \times \text{Number of XHS pulses per frame} - 43\}$	Global reset shutter mode (SMD = 1)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

Note)

- See "Integration Time in Each Readout Drive Mode" on page 97 for the integration time calculation formula.
- The SVR register setting range is guaranteed only as sensor function, characteristics are not guaranteed.
- SMD is the electronic shutter drive mode register (address 3008h, bit [0]).

1-2. Electronic Shutter Drive Mode (CSI-2)

Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD.

Rolling shutter operation performs pixel reset and integration sequentially in line units. Global reset shutter operation resets all pixels at once and then starts integration after that.

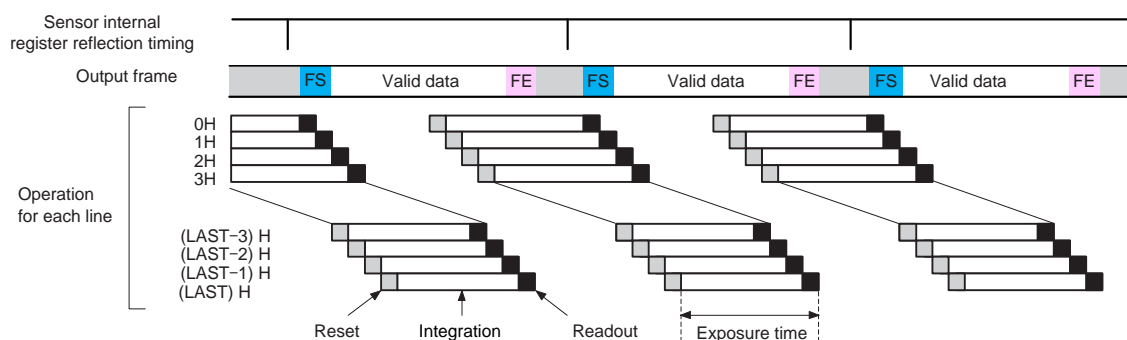
(“Integration” is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.) The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.

Using XVS output sync signal from sensor as trigger signal is recommended in the case of synchronizing global reset shutter timing of sensor and mechanical shutter timing outside of sensor is needed for fine adjustment of integration time.

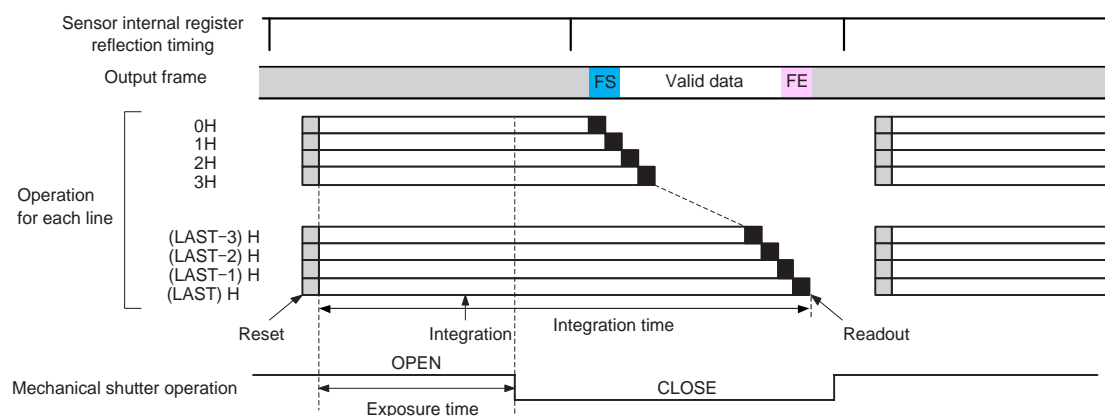
Consult your Sony sales representative concerning to use XVS output signal.

SMD Setting

Name	CSI-2 (I ² C) Address	Bit	Register value	Function
SMD	3008h	[0]	0h	Rolling shutter (normal shutter mode)
			1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

2. Integration Time in Each Readout Drive Mode and Mode Changes When Using CSI-2

2-1. Integration Time in Each Readout Drive Mode (CSI-2)

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR and SVR. The formulas and constants used to calculate the integration time are shown below. In addition, the frame rate can be reduced by setting the SVR register to "1" or more.

◆ Integration time of normal readout drive mode (other than mode No.11)

$$\text{Integration Time [s]} = \{[\text{VMAX value} \times (\text{SVR value} + 1) - \text{SHR value}] \times \text{HMAX value} + \text{Number of clocks per internal offset period}\} / (72 \times 10^6)$$

* See the following tables for the numbers of clocks per internal offset period.

* See "Electronic Shutter Timing" on page 95 of the SHR register setting range.

◆ Integration time of normal readout drive mode No.11

$$\text{Integration Time [s]} = \{[\text{VMAX value} \times (\text{SVR value} + 1) - \text{SHR value} \times 4] \times \text{HMAX value} + \text{Number of clocks per internal offset period}\} / (72 \times 10^6)$$

* See the following tables for the numbers of clocks per internal offset period.

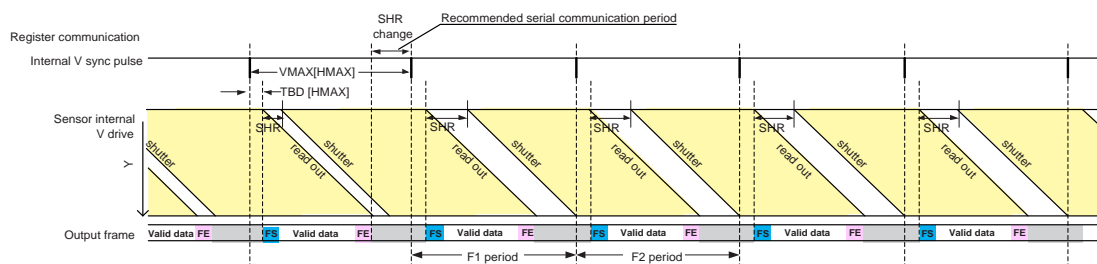
* See "Electronic Shutter Timing" on page 95 of the SHR register setting range.

Number of clocks per internal offset period

Readout mode No.	0	1	1A	1B	2	2A	3	4	5	6	7	8	9	10	11
Number of clocks per internal offset period	551	256	361	256	217	322	256	256	217	217	217	217	217	217	217

The figure below shows operation when SHR is being changed and REGHOLD is 0h. The F1 and F2 periods in the figure below are two continuous frames. The SHR value which is set in the recommended serial communication period^{*1} just before F1 period is updated internally at the end of the communication period and then output data which reflect the new setting is output in the F2 period. Note that the SHR setting and output are offset by a frame.

^{*1} Refer to "Register Communication Timing" on page 35.

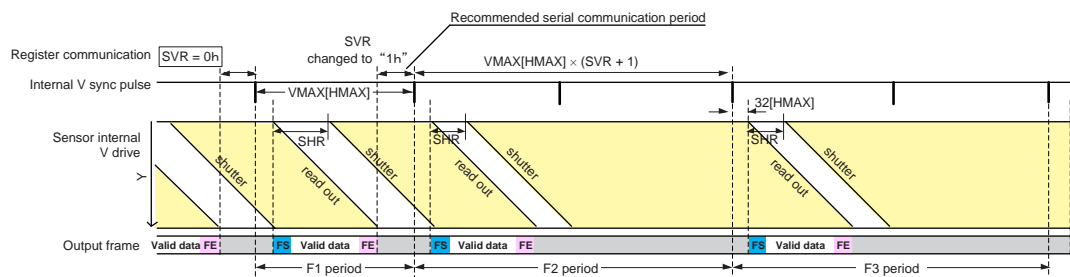


SHR Change Sequence (CSI-2)

The internal vertical drive period which is set by the VMAX register can be subsampled by the SVR register. Its period is (SVR value + 1) times as long as VMAX period. Therefore the frame rate is multiplied by $1 / (\text{SVR value} + 1)$. The figure below shows the operation when the SVR register is being changed from "0h" to "1h" and REGHOLD is 0h. The SVR value, which is set in the recommended serial communication period^{*1} just before F2 period, is updated internally at the end of the communication period and then applied from the shutter operation in the F2 period. The output data which reflect the changing of SVR is output in the F3 period.

The image data of the F1 period before the SVR value is changed is output as valid data in the F2 period.

^{*1} Refer to "Register Communication Timing" on page 35.



SVR Change Sequence (CSI-2)

2-2. Operation when Changing the Readout Drive Mode (CSI-2)

When changing input INCK or CSI-2 output frequency, follow the below procedure.

- 1st step: Enter the sensor standby mode
- 2nd step: Change the frequency during standby mode.
- 3rd step: Follow the standby cancel sequence to resume the normal operation.

When changing input INCK frequency, don't input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low. Then set the state of XCLR to High, following the item of "Power on sequence" in the section of "Power on / off sequence" in page 141. Execute "Standby Cancel Sequence" again because the register settings become default state after system reset.

The following mode change cases are treated as a mode transition on this sensor and one frame of invalid data is generated.

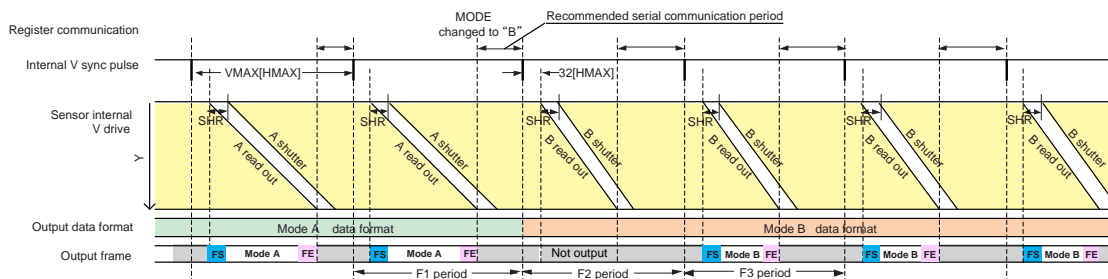
1. Changing the readout mode setting
2. Changing the vertical direction readout setting
3. Changing the vertical arbitrary cropping setting
- * Changing the horizontal arbitrary cropping setting is not treated as mode transition and no invalid data is generated.

The figure below shows the mode transition sequence, Mode A to Mode B, in case that the mode transition is performed in three continuous frames, F1 to F3, and REGHOLD is 0h.

- (1) Set the register setting for Mode B in the recommended serial communication period^{*1} just before F2 period. The F2 period data is not output.
- (2) Valid data which reflect the new setting is output from the next frame (F3 period).

^{*1} Refer to "Register Communication Timing"

In addition, note that when the output data length differs between Mode A and Mode B, the new data format is output from the start of F2 period in which the setting is changed to Mode B.



Mode Transition (CSI-2)

Image Data Output Format When Using SLVS-EC

Line Format and Frame Format (Sync Signals and Data Output Timing) (SLVS-EC)

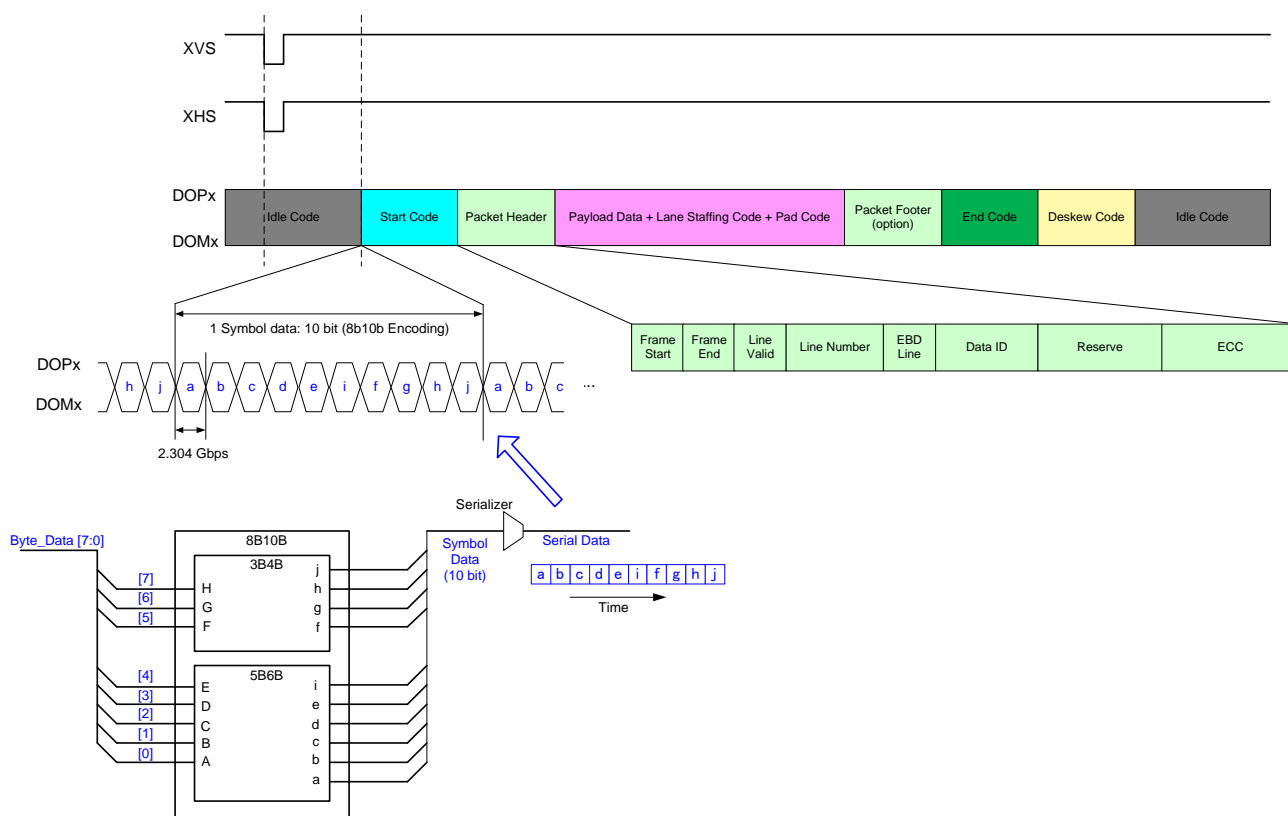
The format of each line and each frame of this sensor are described below.

The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals.

Timing control is performed at the falling edge of both the XVS and XHS signals.

Line Format

The figure below shows the line format of each line. 1 Symbol consists of 10 bits regardless of readout drive mode. Refer to "SLVS-EC Specification" for detail.



Line Format

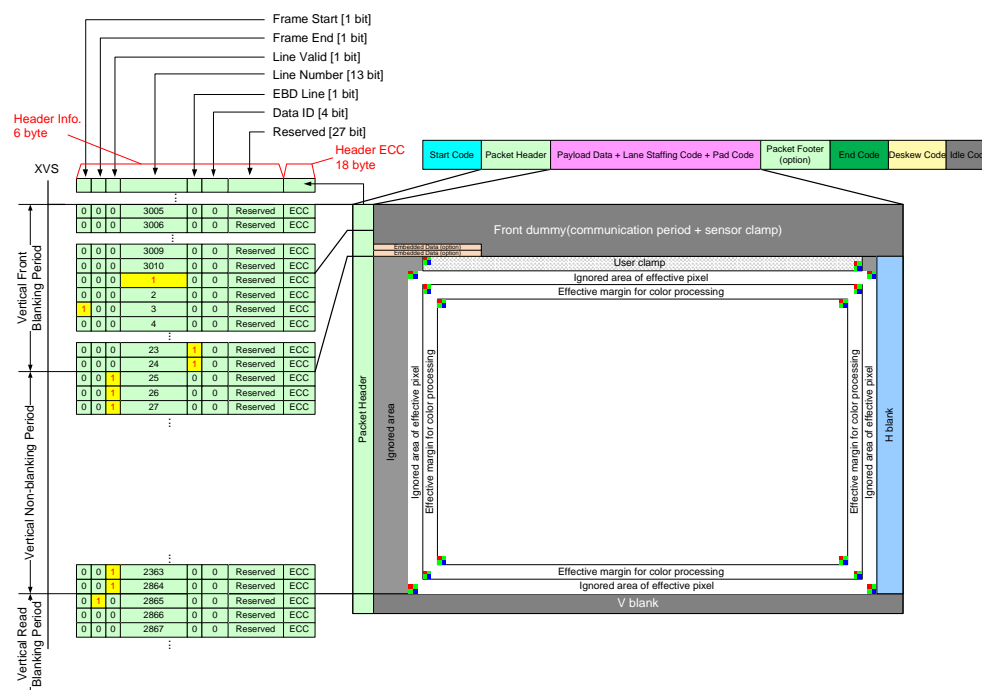
Frame Format (SLVS-EC)

In this section the frame formats in following cases are described.

1. Normal frame
2. Invalid frame (with training sequence)
3. Invalid frame (without training sequence)

1. Normal frame

As an example, the figure below shows XVS timing and contents of the header in each line in the case of readout mode No. 0, all-pixel scan (14-bit).



Frame Format (Normal frame, in the case of readout mode No.0, All-pixel scan (14 bits))

Contents of Header

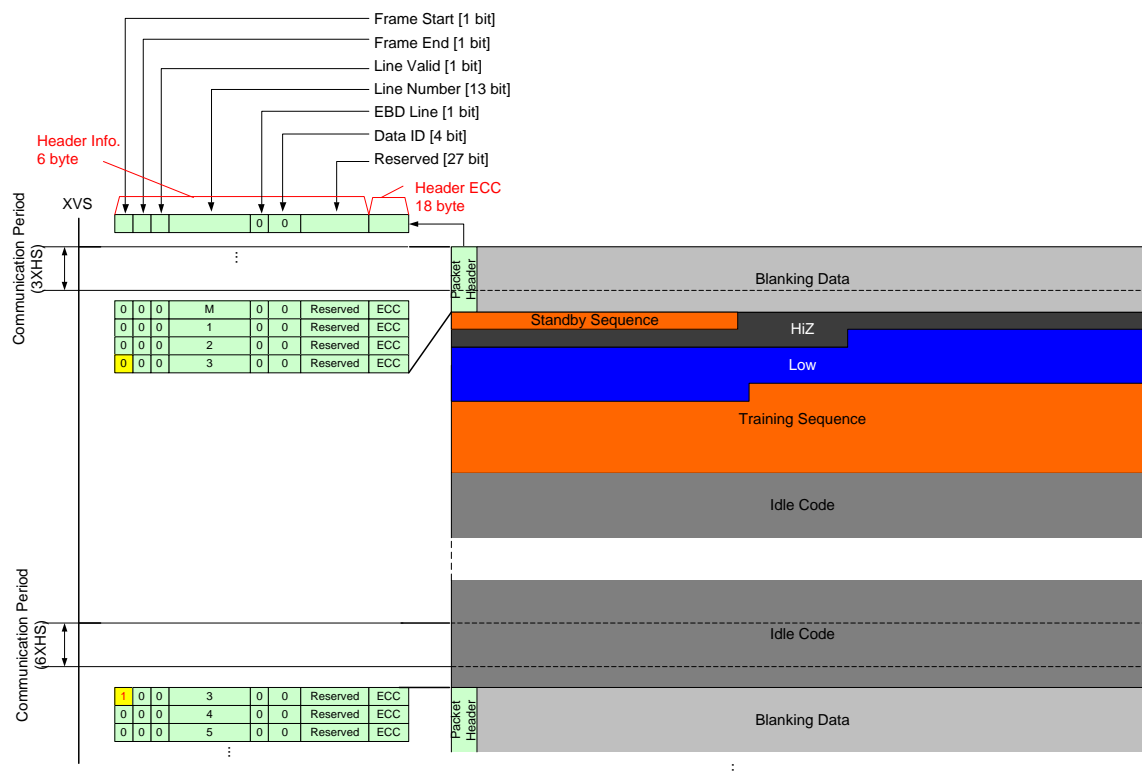
Item	Function
Frame Start	1 is output when Line Number = 3d. (In all readout drive mode)
Frame End	1 is output at the top line of vertical blanking period. In the case when XVS period is short and XVS pulse is input before Frame End outputs 1, Frame End = 1 is output at the same line of Line Number = 1.
Line Valid	Continuously outputs 1 during vertical non-blanking period. In the case when XVS period is short and XVS pulse is input before Frame End outputs 1, Line Valid keeps 1 until the line before the line of Line Number = 1.
Line Number	Line Number is reset to 1 while blanking period in the top of the frame, and incremented by 1 until next reset timing. Its max value is 8191 and stops incrementing after reaching max. (Keeps outputting the same value)
EBD Line	EBD Line = 1 is output in the line of embedded data.
Data ID	Data ID = 0 is output with a drive mode other than HDR. When use HDR function, see the document "IMX294 Application Quad Bayer Coding HDR" for details.

During the recommended serial communication period (3XHS) sequel of the frame before is output, and Line Number is reset to 1 after that. The timing when Line Number is reset to 1 varies with readout drive mode. (See Readout Drive Timing)

Frame Start = 1 is output in the line of Line Number = 3. When the register EBDDATAEN = 1, embedded data is output in the last 2 line of vertical front blanking period (the 2 lines just before the user clamp output). The length of vertical front blanking period is the same with or without embedded data output.

2. Invalid frame (with training sequence)

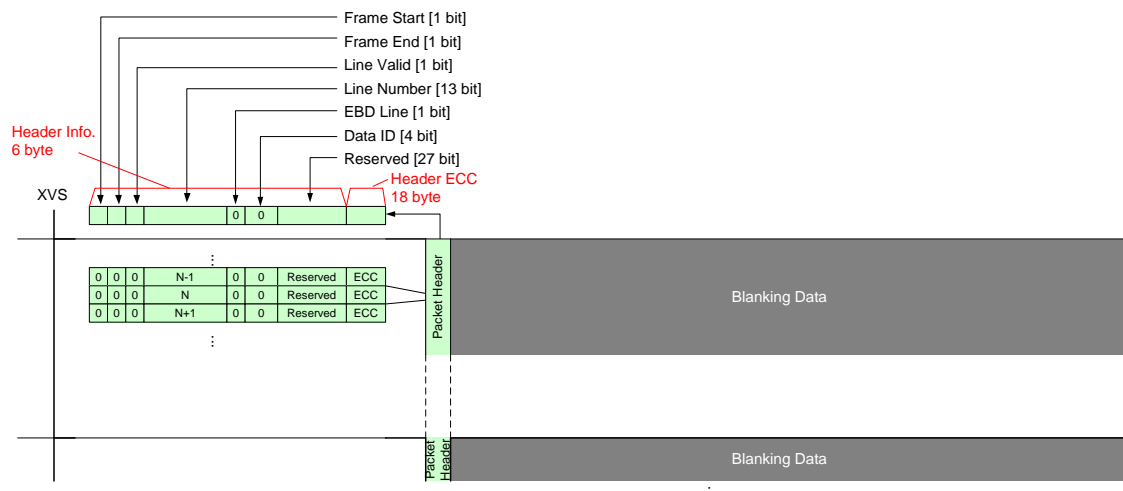
This sensor generates training sequence in standby canceling, mode changing, and so on. From 1 line after the timing of the line that 1 is output in Frame Start in normal frame, standby sequence, low period, training sequence, idle codes are output. During this, Start Code, Packet Header and End Code are not output.



Frame Format (Invalid frame with training sequence)

3. Invalid frame (without training sequence)

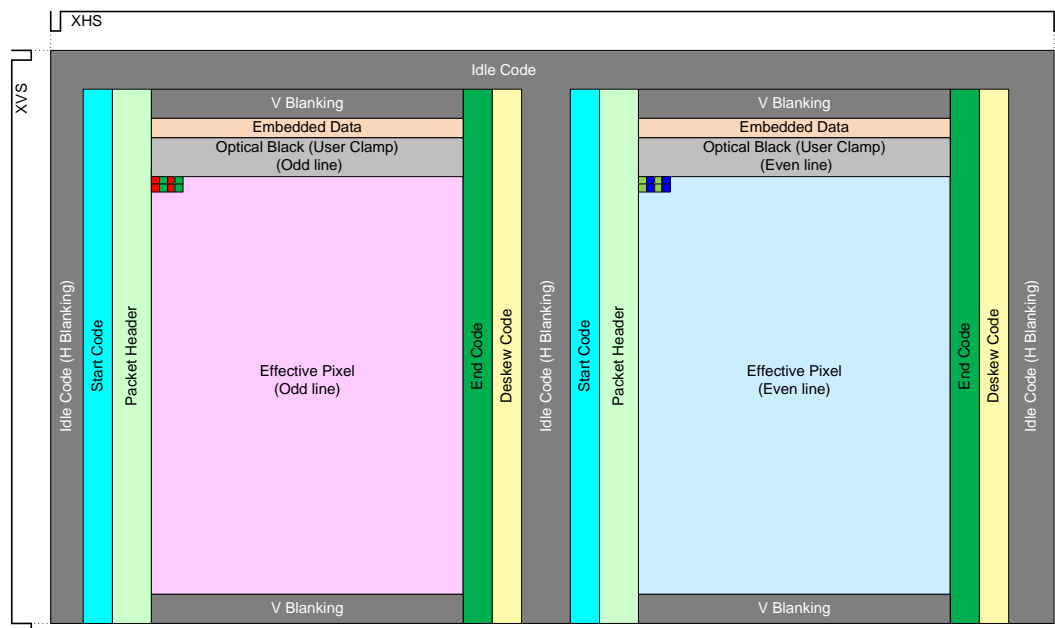
During XVS-subsampled period by SVR, this sensor generates invalid frame without training sequence. Frame Start = 1 and Frame End = 1 is not output in this frame, and Line Number is not reset also.



Frame Format (Invalid frame without training sequence)

Data Output Format (SLVS-EC)

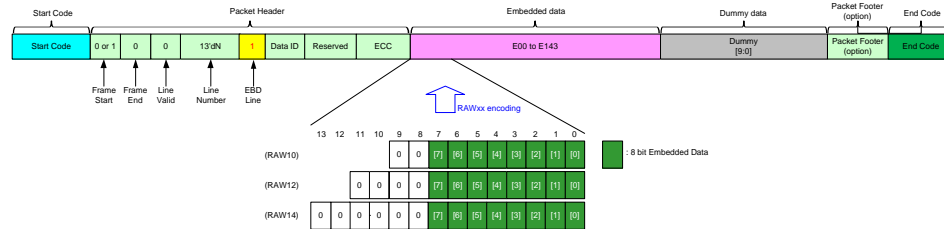
The figure below shows the data output format.
Data output of the two lines in the period of 1XHS.



Data Output Format (SLVS-EC)

Embedded Data (Information Embedding in Images) (SLVS-EC)

When setting the register EBDDATAEN = 1h, embedded data is transferred in 2 lines just before user clamp area. Embedded data output format is shown below. Data of 2 line are same each other. Embedded data consists of 8 bits × 144, but the same encoding format with the image is used by padding 0 to upper bits as necessary. For example, when output bit length of the image is 12 and RAW12 encoding is used, in embedded data block, data of 12 bits × 144 in which 8 bits × 144 of E00 to E143 is LSB aligned are output with RAW12 encoding.



Embedded Data (Information Embedding in Images)

Register Map

Output timing	bit	Transfer data	Description
E00	[2:0]	LANESEL	
	[7:3]	—	(Ignored)
E01 to E05	[7:0]	—	(Ignored)
E06	[0]	SMD	
	[7:1]	—	(Ignored)
E07	[7:0]	PGC	
E08	[2:0]	—	(Ignored)
	[7:3]	—	(Ignored)
E09	[7:0]	SHR	
E10	[7:0]	SHR	
E11	[7:0]	SVR	
E12	[7:0]	SVR	
E13 to E14	[7:0]	—	(Ignored)
E15	[3:0]	DGAIN	
	[4]	MDVREV	
	[7:5]	—	(Ignored)
E16 to E20	[7:0]	—	(Ignored)
E21	[7:0]	BLKLEVEL	
E22	[1:0]	—	(Ignored)
	[7:2]	—	(Ignored)
E25	[0]	HTRIMMING_EN	
	[7:1]	—	(Ignored)
E26	[7:0]	HTRIMMING_START	
E27	[5:0]	—	(Ignored)
	[7:6]	—	(Ignored)
E28	[7:0]	HTRIMMING_END	
E29	[5:0]	—	(Ignored)
	[7:6]	—	(Ignored)
E30	[0]	VWIDCUTEN	
	[3:1]	—	(Ignored)
	[7:4]	—	(Ignored)
E31	[7:0]	VWINPOS	
E32	[5:0]	—	(Ignored)
	[7:6]	—	(Ignored)
E33	[7:0]	VWIDCUT	
E34	[5:0]	—	(Ignored)
	[7:6]	—	(Ignored)
E35 to E143	[7:0]	—	(Ignored)

Detailed Specification of Each Mode (SLVS-EC)

1. When Using Aspect Ratio Approx. 17:9 (Approx. 9.07 M pixels)

1-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (SLVS-EC)

Horizontal Operation Period in Each Readout Drive Mode (SLVS-EC)

Readout mode No.	Horizontal operation period (Number of pixels conversion)						XHS minimum period [INCK] ^{*1*2}	XHS number per H period
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel		
1	0	24	12	4096	12	0	725	0.5
1A	0	24	12	4096	12	32	1192	0.5
2	0	24	12	4096	12	0	520	0.5
2A	0	24	12	4096	12	32	827	0.5
3	0	12	6	2048	6	16	706	1
4	0	12	6	2048	6	16	706	1
5	0	12	6	2048	6	16	520	1
6	0	12	6	2048	6	16	520	1
7	0	12	6	2048	6	16	520	0.5
8	0	8	4	1364	4	12	520	1.5
9	0	8	4	1364	4	12	520	0.5
10	0	8	4	1364	4	12	743	1
11	0	8	4	1364	4	12	520	4

^{*1} Number of clocks in conversion of INCK = 72 MHz.

^{*2} If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.

Vertical Operation Period in Each Readout Drive Mode (SLVS-EC)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)							XVS minimum period [XHS]
	Vertical front blanking	Front OB (User Clamp)	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
1	24(15XHS)	8	8	4	2160	4	0	1107
1A	24(15XHS)	8	8	4	2160	4	0	1107
2	24(15XHS)	8	8	4	2160	4	0	1107
2A	24(15XHS)	8	8	4	2160	4	0	1107
3	11(15XHS)	4	4	6	1080	6	0	1115
4	6(9XHS)	4	4	6	1080	6	0	1109
5	11(15XHS)	4	4	6	1080	6	0	1115
6	6(9XHS)	4	4	6	1080	6	0	1109
7	12(9XHS)	4	4	6	1080	6	0	559
8	9(21XHS)	4	4	6	720	6	0	1131
9	12(9XHS)	4	4	6	720	6	0	379
10	11(15XHS)	4	4	2	240	2	0	267
11	6(27XHS)	4	2	2	240	2	0	257

1-2. Frame Rate Adjustment (SLVS-EC)

The formula for frame rate calculation is shown below.

$$\text{Frame rate [frame/s]} = (72 \times 10^6) / \{ \text{XHS period [INCK]} \times \text{XVS period [XHS]} \times (\text{SVR register value} + 1) \}$$

The frame rate can be changed by changing XHS period and XVS period as long as these are set to minimum value or larger. Larger XHS period results in longer horizontal blanking period. Larger XVS period results in longer vertical blanking period. The examples of setting for each readout drive mode are shown in the table below. Set XHS period and XVS period considering ISP image processing time.

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See "Electronic Shutter Timing" on page 133 for details.

Examples of XHS Period, XVS period and Frame Rate (SLVS-EC)

Readout mode No.	XHS min period (INCK) ^{*1}	XVS min period (number of XHS pulses)	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				XHS period (INCK) ^{*1}	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]	XHS period (INCK) ^{*1}	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]
1	725	1107	89.71	728	1650	0	59.94	800	1800	0	50.00
1A	1192	1107	54.56	1200	2002	0	29.97	1250	2304	0	25.00
2	520	1107	125.08	520	1155	0	119.88	576	1250	0	100.00
2A	827	1107	78.65	840	1430	0	59.94	900	1600	0	50.00
3	706	1115	91.46	715	1680	0	59.94	720	2000	0	50.00
4	706	1109	91.96	715	1680	0	59.94	720	2000	0	50.00
5	520	1115	124.18	520	1155	0	119.88	576	1250	0	100.00
6	520	1109	124.85	520	1155	0	119.88	576	1250	0	100.00
7	520	559	247.70	525	572	0	239.76	576	625	0	200.00
7 (60fps)				525	572	3	59.94	576	625	3	50.00
8	520	1131	122.42	520	1155	0	119.88	576	1250	0	100.00
8 (30fps)				520	1155	3	29.97	576	1250	4	25.00
9	520	379	365.33	520	462	0	299.70	576	500	0	250.00
9 (60fps)				520	462	4	59.94	576	500	4	50.00
10	743	267	362.94	770	312	0	299.70	800	360	0	250.00
10 (60fps)				770	312	4	59.94	800	360	4	50.00
11	520	257	67.35 ^{*2}	525	572	7	29.97	600	600	7	25.00

^{*1} Number of clocks in conversion of INCK = 72 MHz

^{*2} Low power consumption drive (SVR = 7h)

1-3. Imaging Conditions in Each Readout Drive Mode (SLVS-EC)

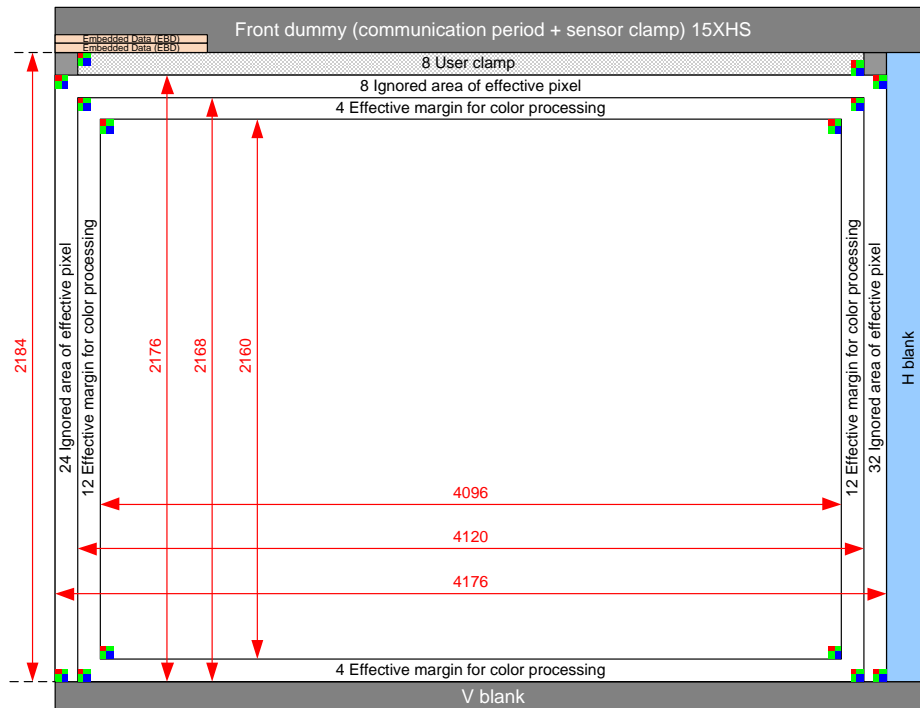
Readout mode No.	Imaging conditions					
	Number of SLVS-EC output channels [lane]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
1	6	12	12	4096	2160	Approximately 8.85 M Pixels
1A	6	12	12	4096	2160	Approximately 8.85 M Pixels
2	8	10	10	4096	2160	Approximately 8.85 M Pixels
2A	6	10	10	4096	2160	Approximately 8.85 M Pixels
3	4	12	14	2048	1080	Approximately 2.21 M Pixels
4	4	12	12	2048	1080	Approximately 2.21 M Pixels
5	6	10	12	2048	1080	Approximately 2.21 M Pixels
6	4	10	10	2048	1080	Approximately 2.21 M Pixels
7	4	10	10	2048	1080	Approximately 2.21 M Pixels
8	4	10	12	1364	720	Approximately 0.98 M Pixels
9	4	10	12	1364	720	Approximately 0.98 M Pixels
10	2	10	12	1364	240	Approximately 0.33 M Pixels
11	1	10	10	1364	240	Approximately 0.33 M Pixels

(SLVS-EC) MODE1: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)

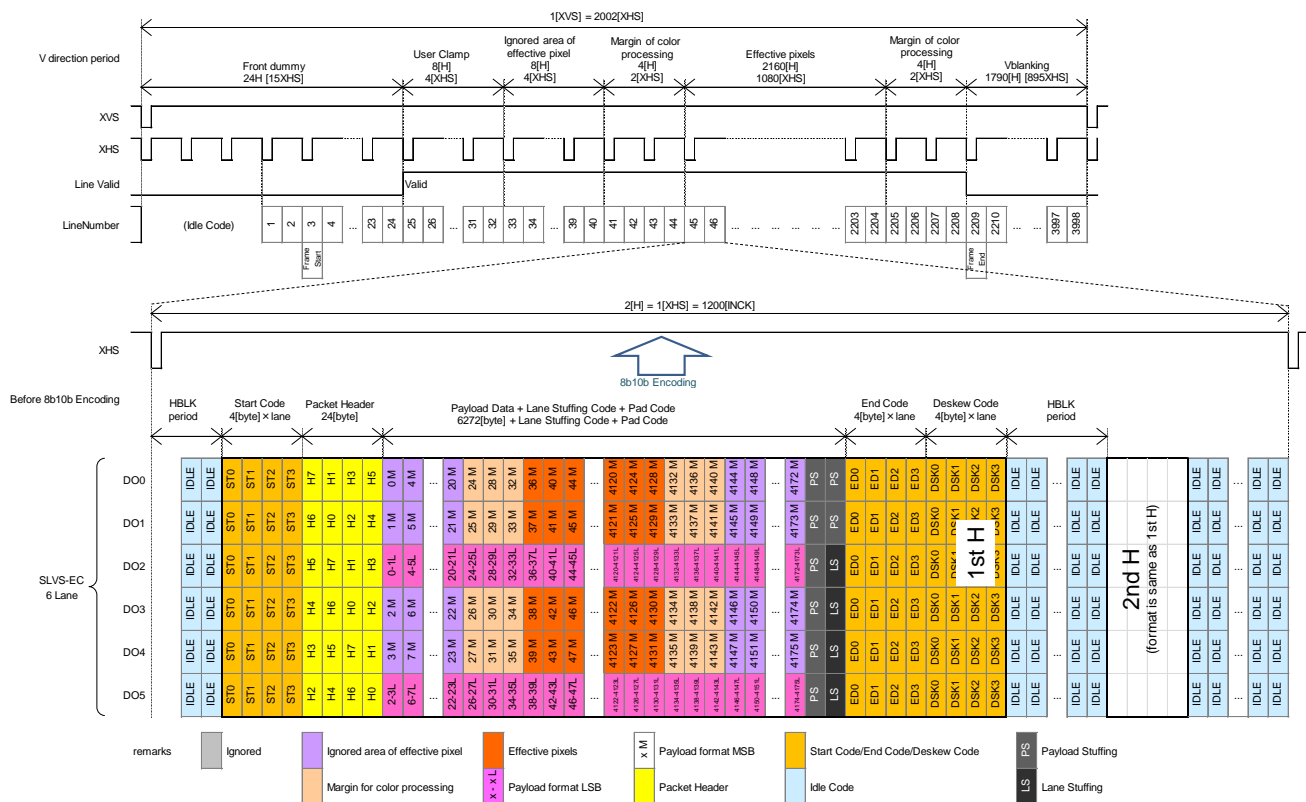


Readout Drive Timing

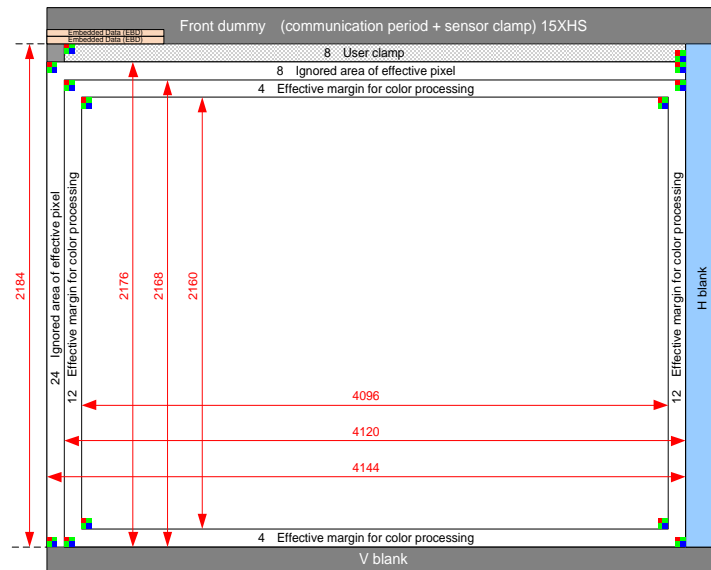
(SLVS-EC) MODE1A: All-pixel scan mode low noise
(12-bit A/D conversion, 12-bit length output)



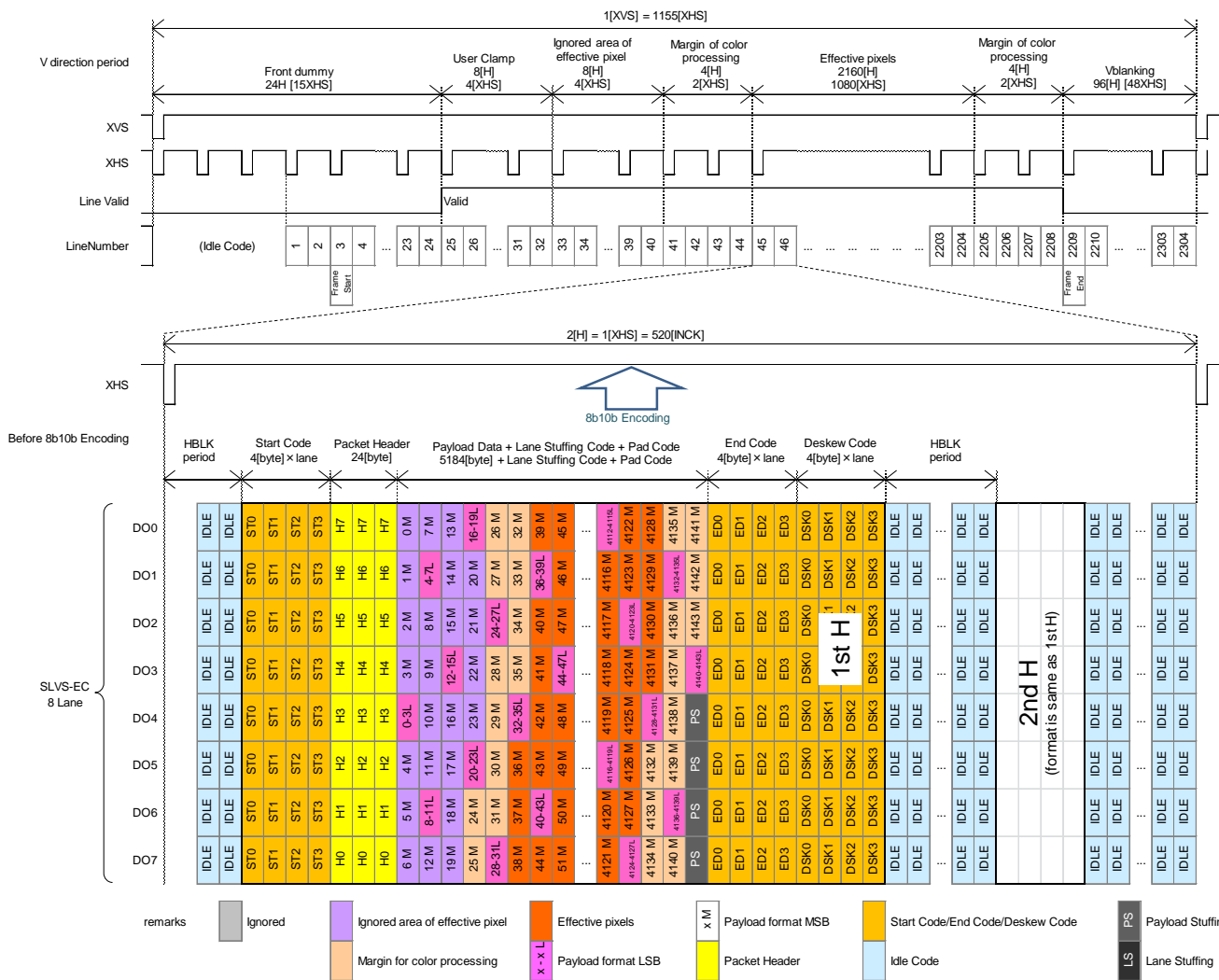
Readout Pixel Image Diagram (4096 × 2160)



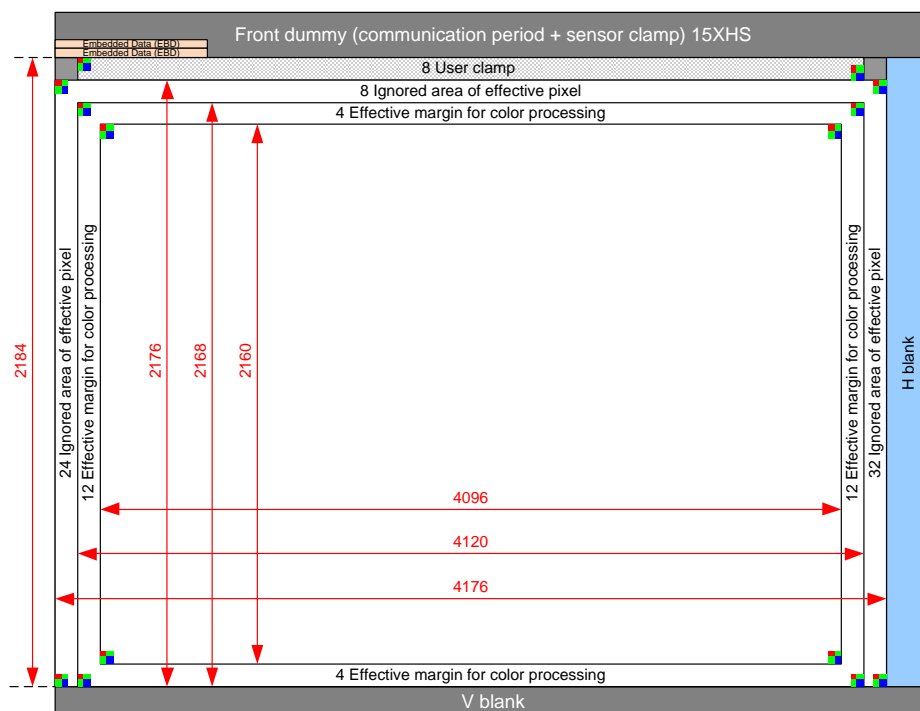
(SLVS-EC) MODE2: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)



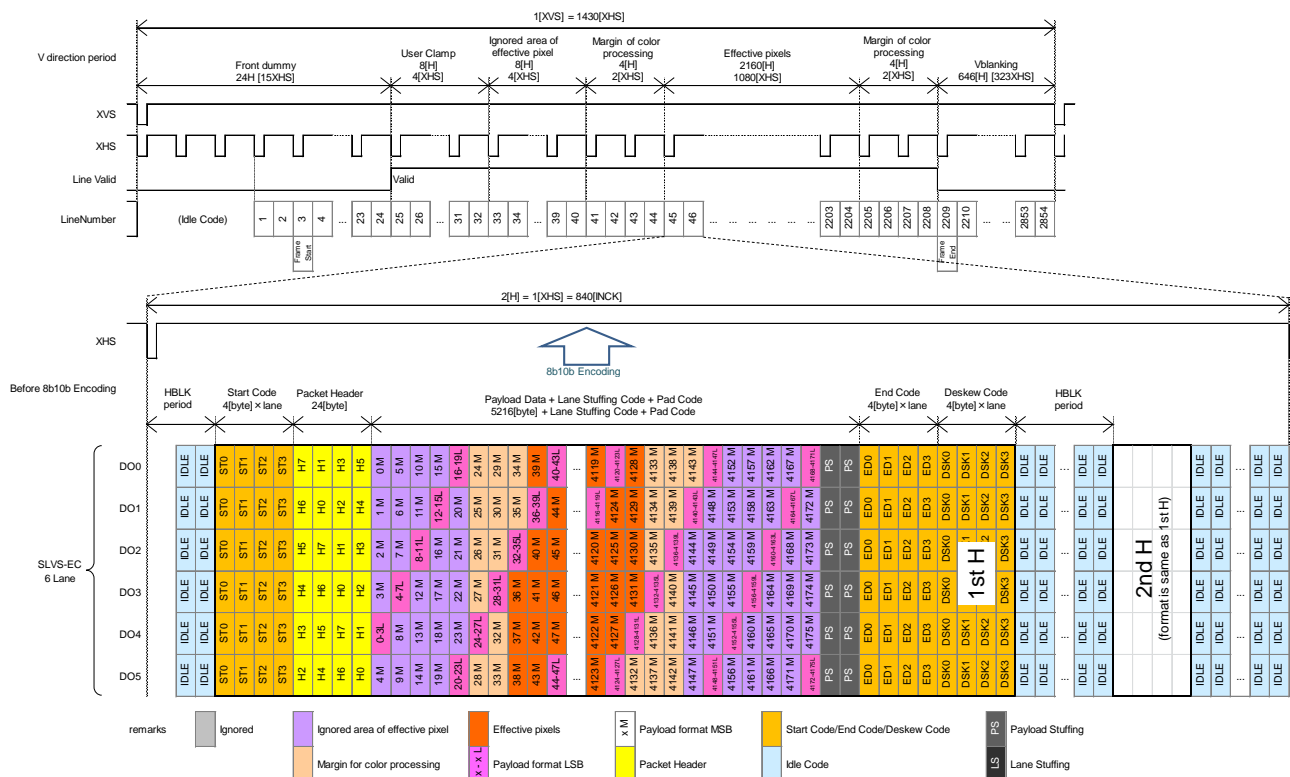
Readout Pixel Image Diagram (4096 × 2160)



(SLVS-EC) MODE2A: All-pixel scan mode low noise
(10-bit A/D conversion, 10-bit length output)

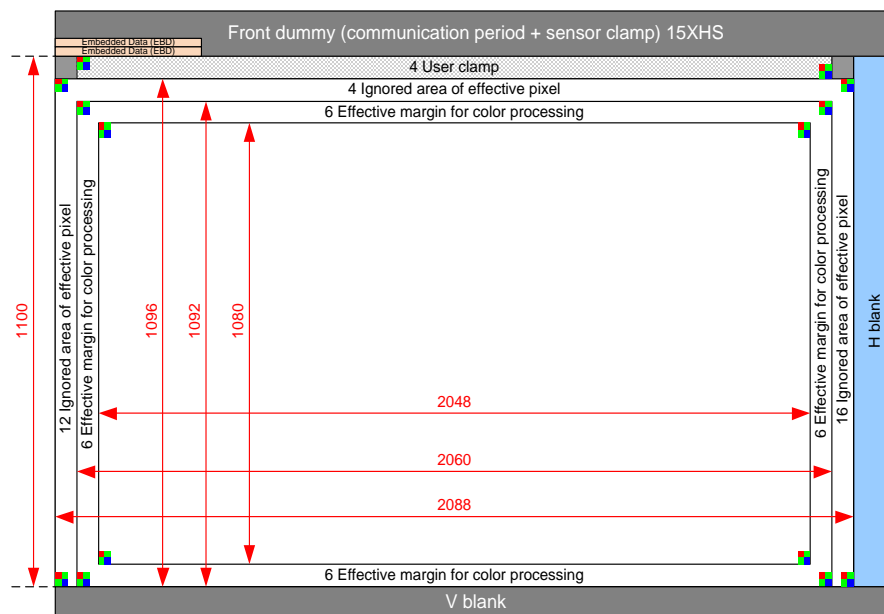


Readout Pixel Image Diagram (4096 x 2160)

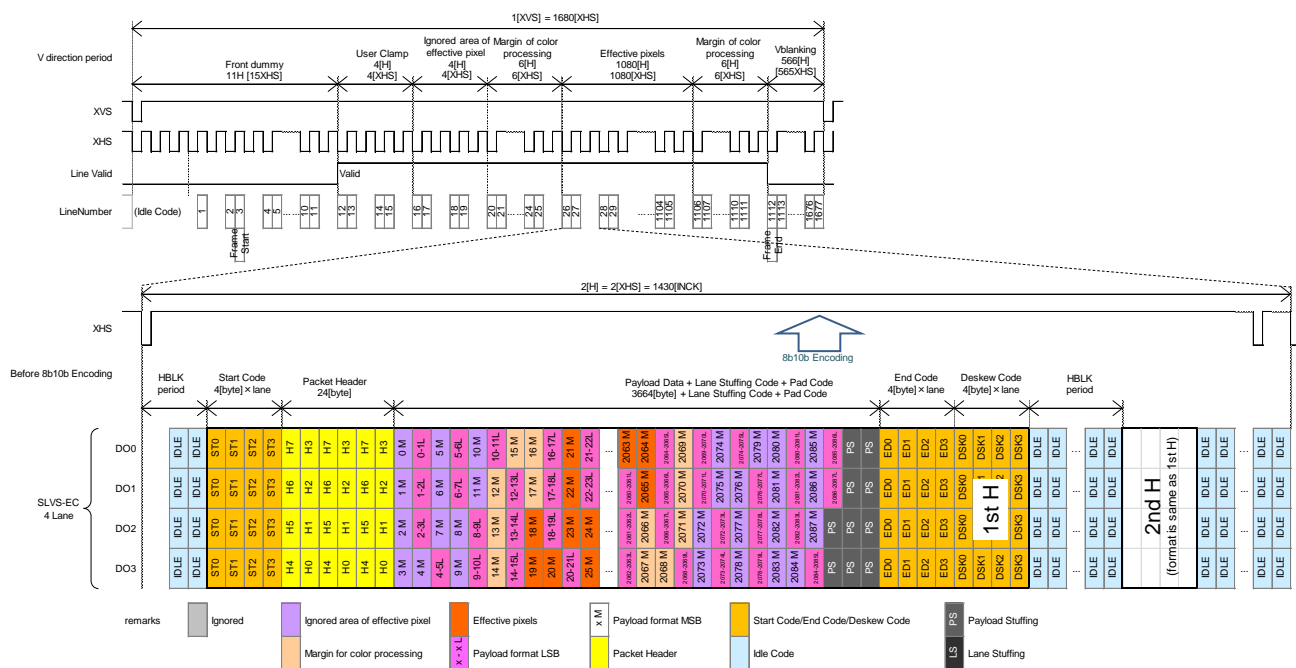


Readout Drive Timing

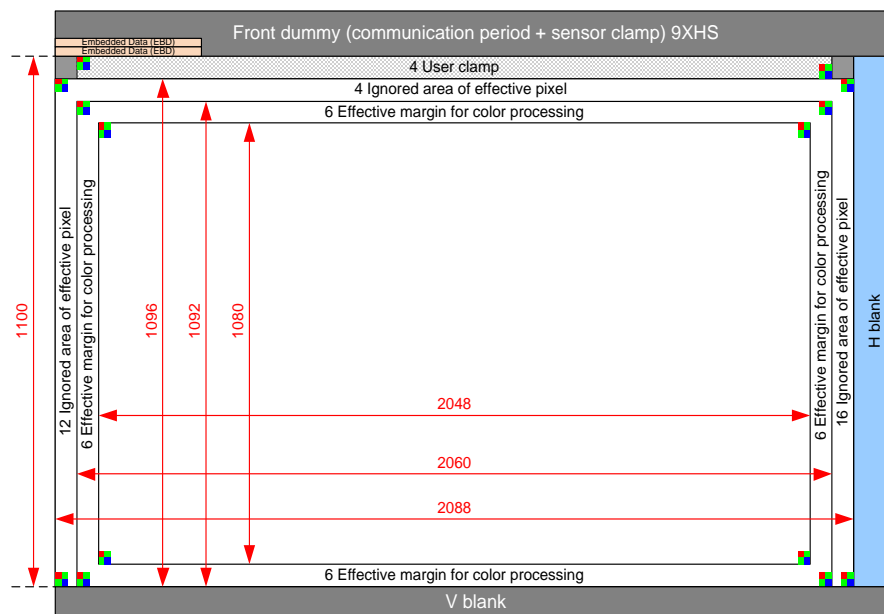
(SLVS-EC) MODE3: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(12-bit A/D conversion, 14-bit length output)



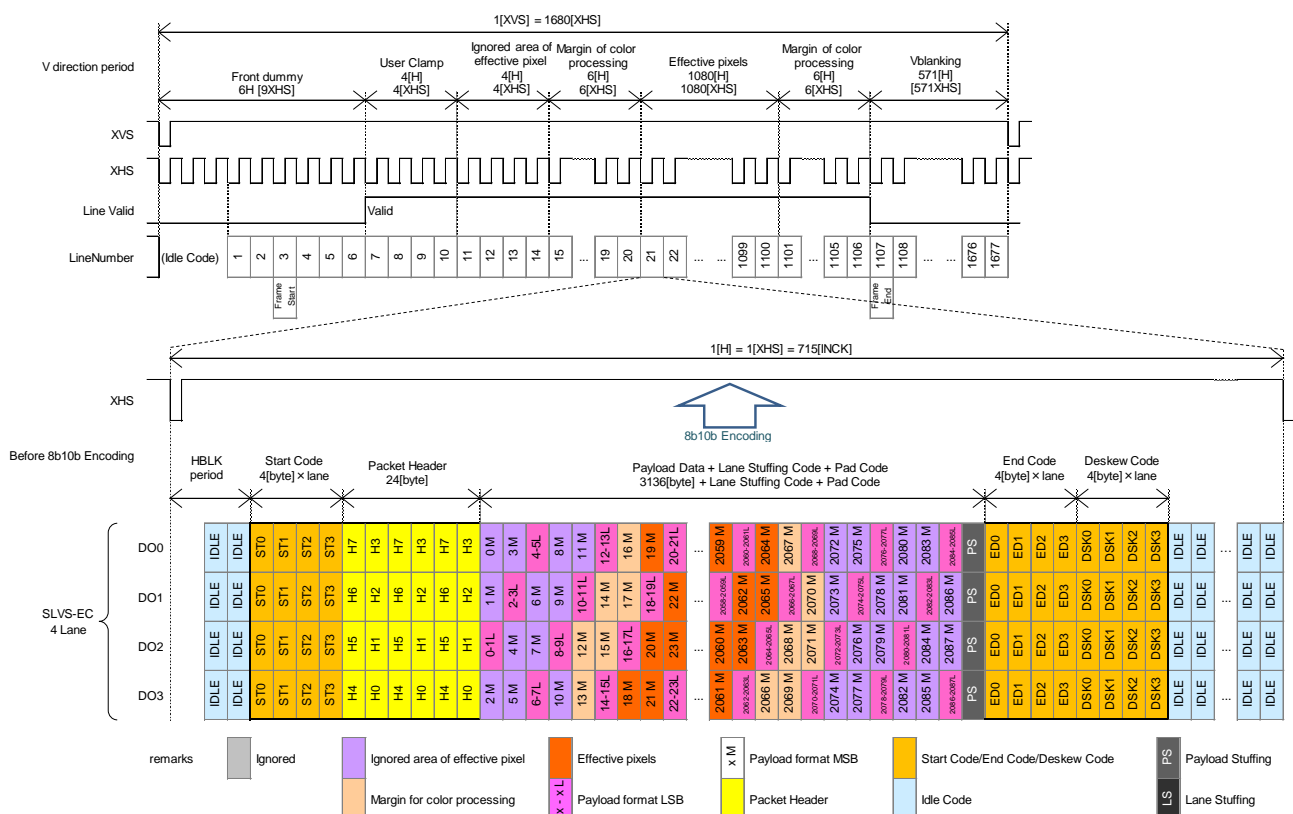
Readout Pixel Image Diagram (2048 x 1080)



(SLVS-EC) MODE4: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(12-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (2048 x 1080)



Front dummy (communication period + sensor clamp) 15XHS

4 User clamp

4 Ignored area of effective pixel

6 Effective margin for color processing

1100

12 Ignored area of effective pixel

6 Effective margin for color processing

16 Ignored area of effective pixel

H blank

2048

2060

2088

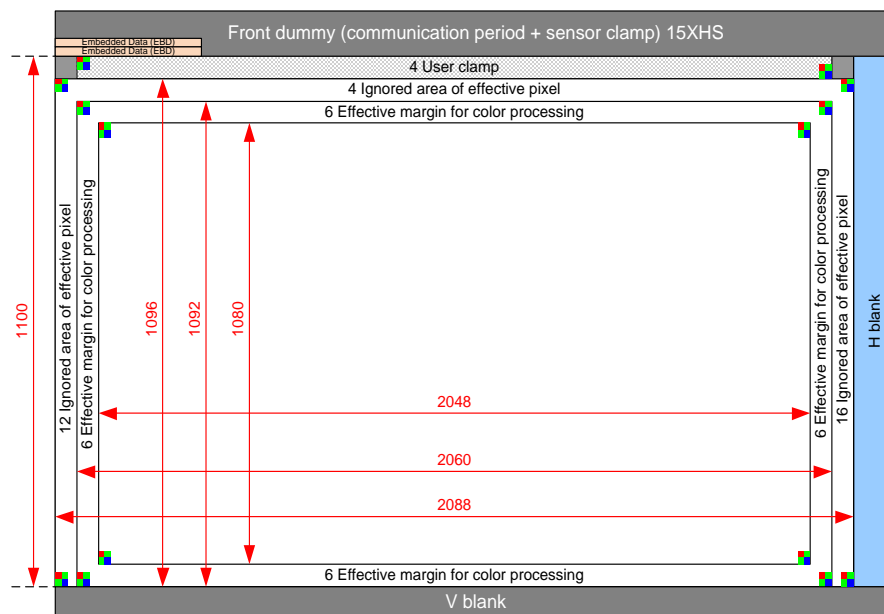
6 Effective margin for color processing

V blank

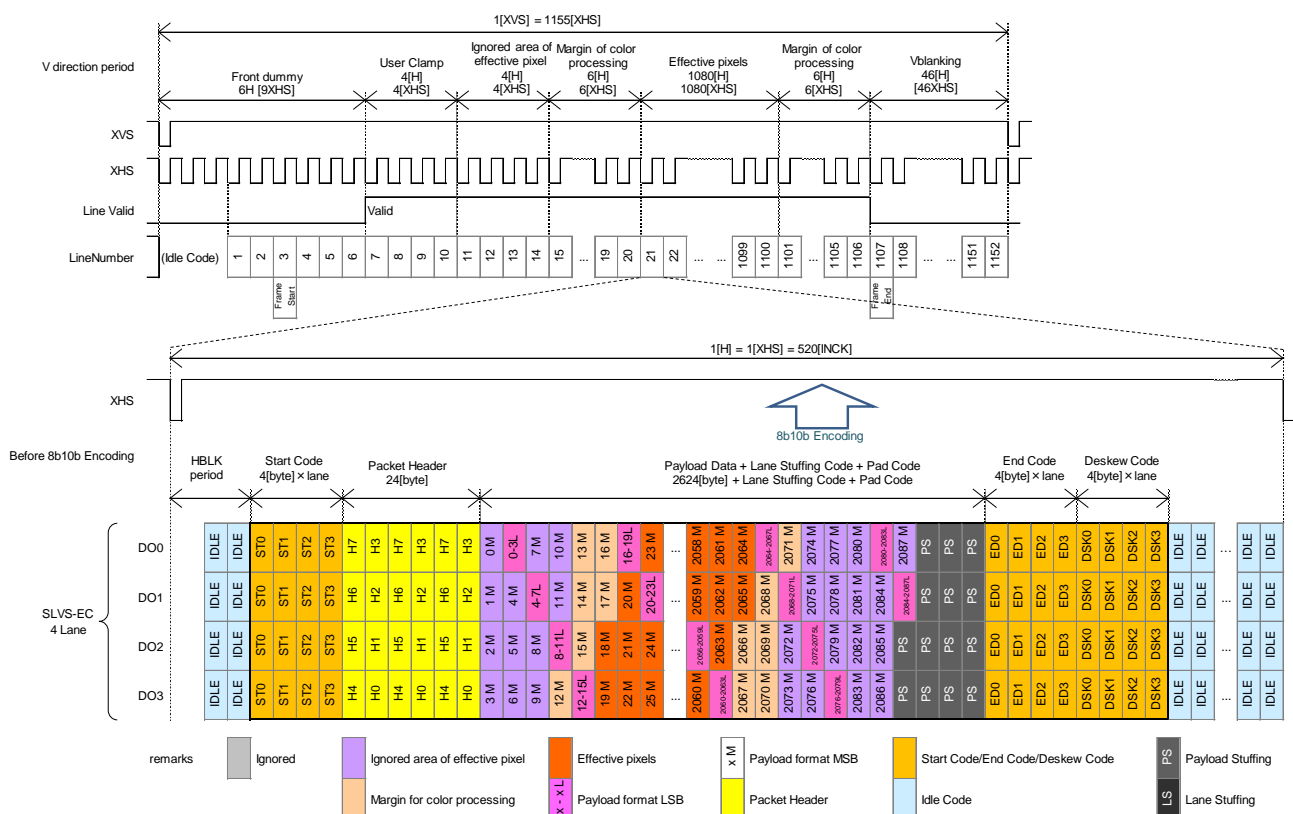
[illegible]

Readout Drive Timing

(SLVS-EC) MODE6: Vertical 2 binning horizontal 2/4 subsampling (vertical weighted binning)
(10-bit A/D conversion, 10-bit length output)

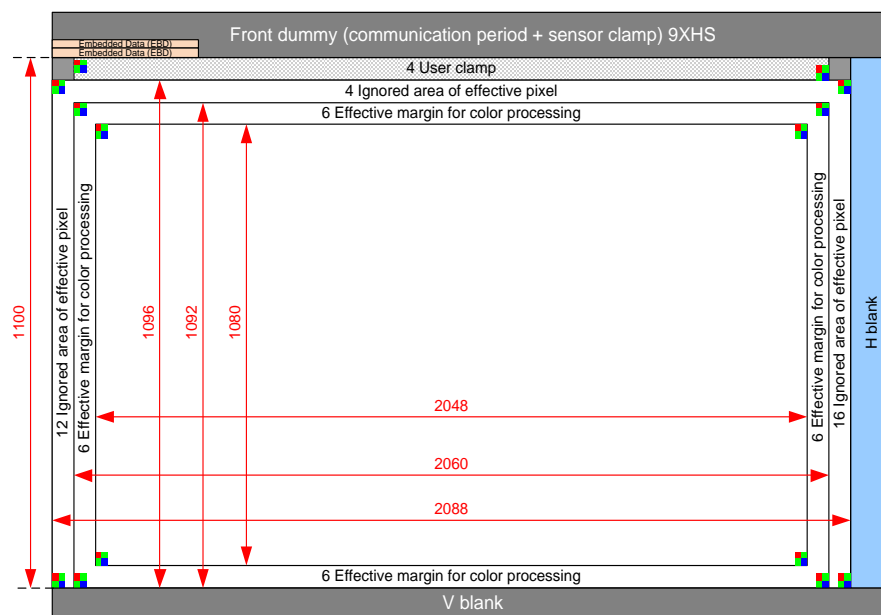


Readout Pixel Image Diagram (2048 × 1080)

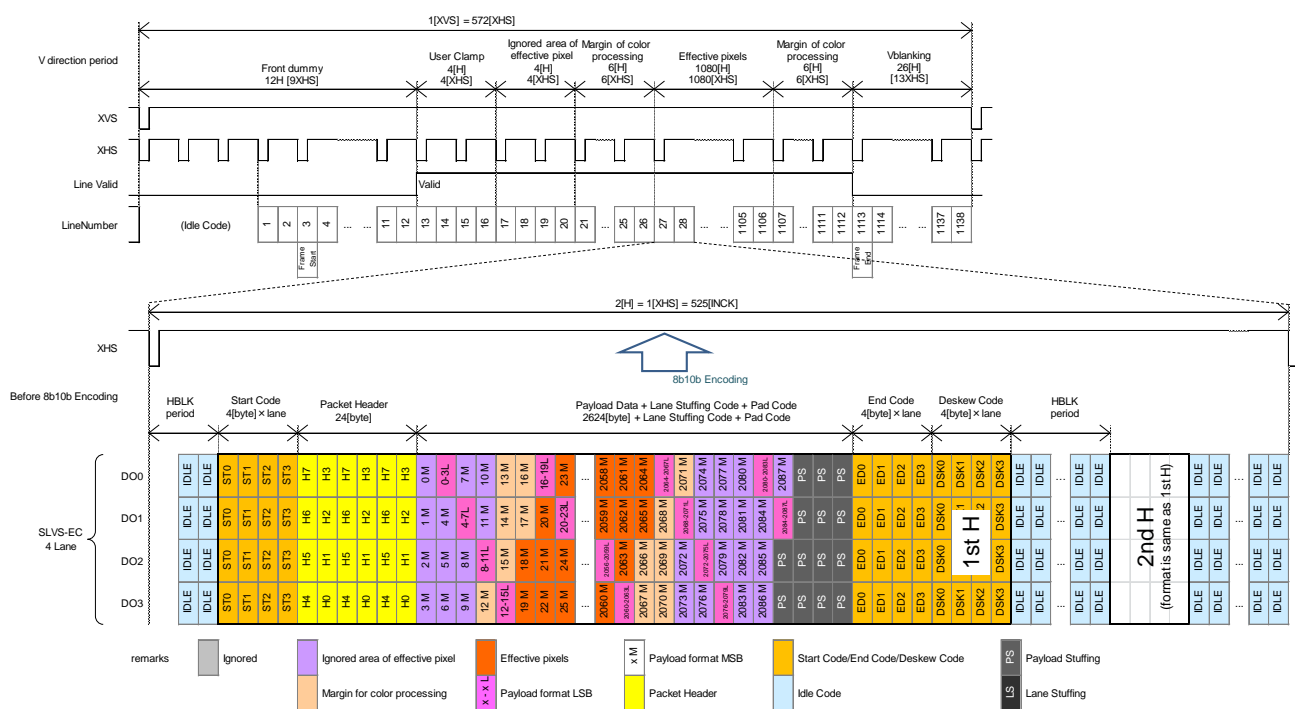


Readout Drive Timing

(SLVS-EC) MODE7: Horizontal/vertical 2/4 subsampling (10-bit A/D conversion, 10-bit length output)



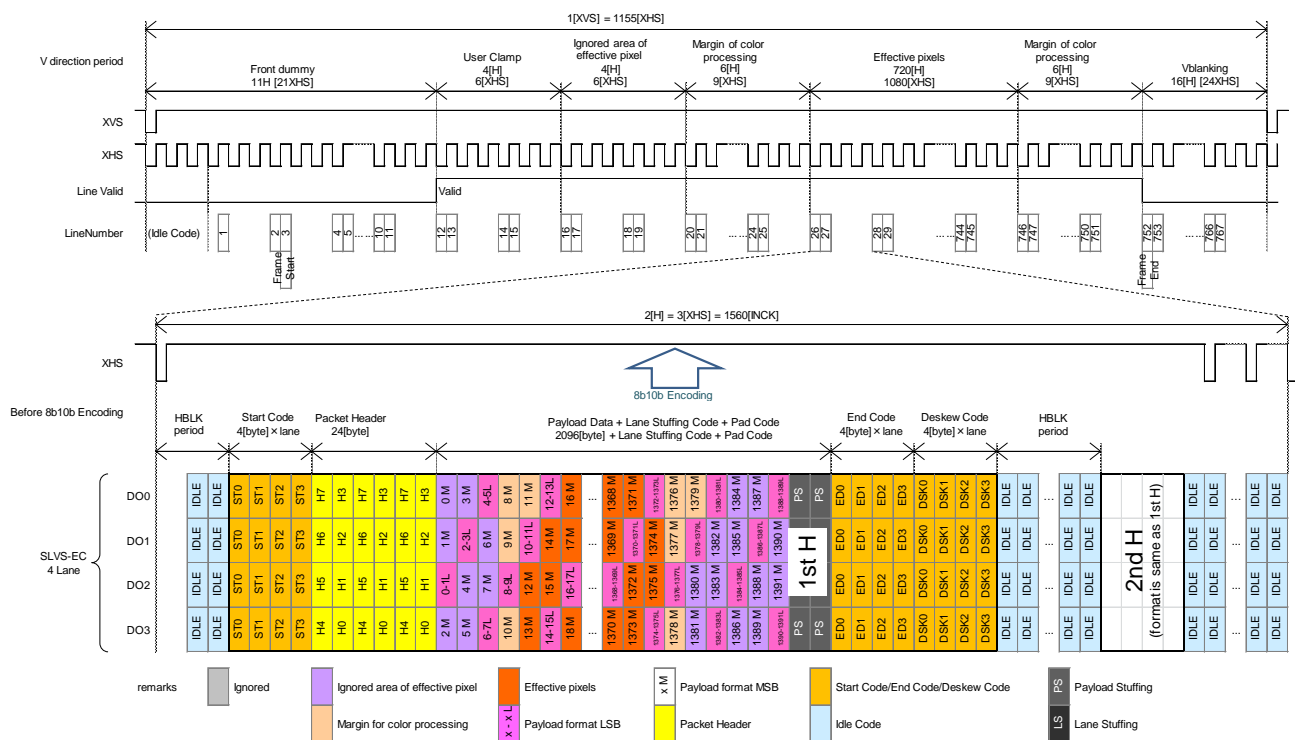
Readout Pixel Image Diagram (2048 × 1080)



The diagram illustrates the 21XHS sensor layout with the following dimensions and margins:

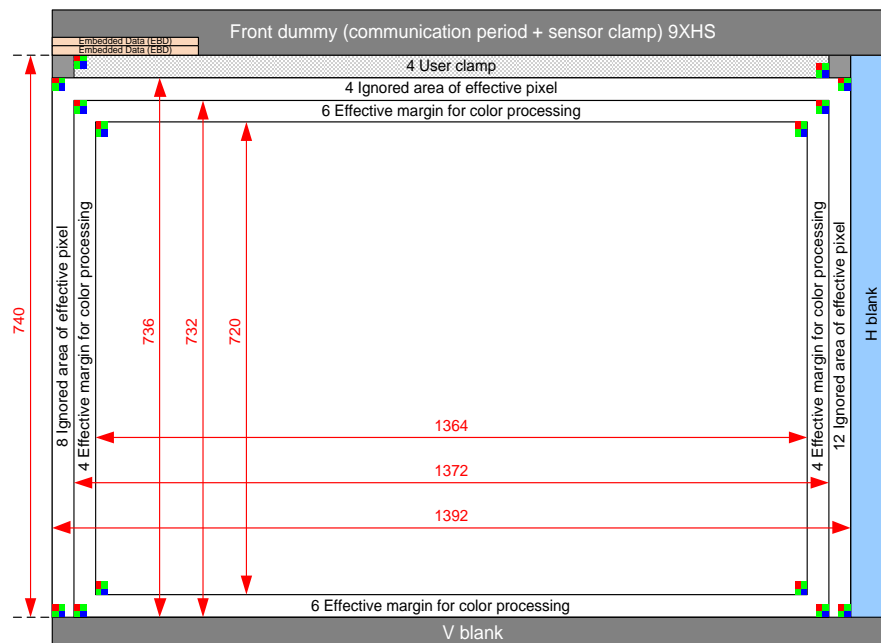
- Top Margins:**
 - Embedded Data (EBD)
 - Embedded Data (EBD)
 - 4 User clamp
 - 4 Ignored area of effective pixel
- Left Margins:**
 - 8 Ignored area of effective pixel
 - 4 Effective margin for color processing
- Right Margins:**
 - 4 Effective margin for color processing
 - 12 Ignored area of effective pixel
 - H blank
- Bottom Margins:**
 - 6 Effective margin for color processing
 - V blank
- Internal Dimensions (Effective Area):**
 - Horizontal: 1364, 1372, 1392
 - Vertical: 736, 732, 720
- Overall Dimensions:**
 - Width: 2148
 - Height: 740

Readout Pixel Image Diagram (1364 x 720)

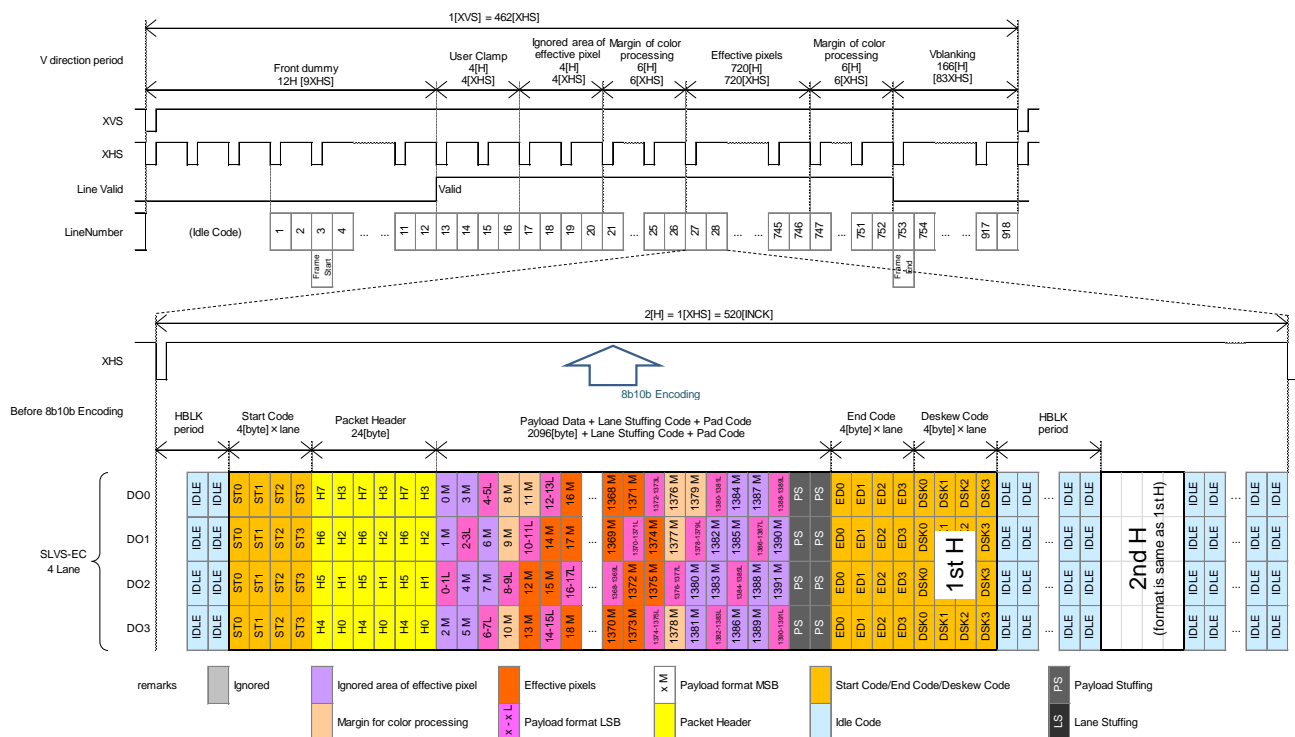


Readout Drive Timing

(SLVS-EC) MODE9: Vertical 1/3 subsampling horizontal 3 binning
(10-bit A/D conversion, 12-bit length output)

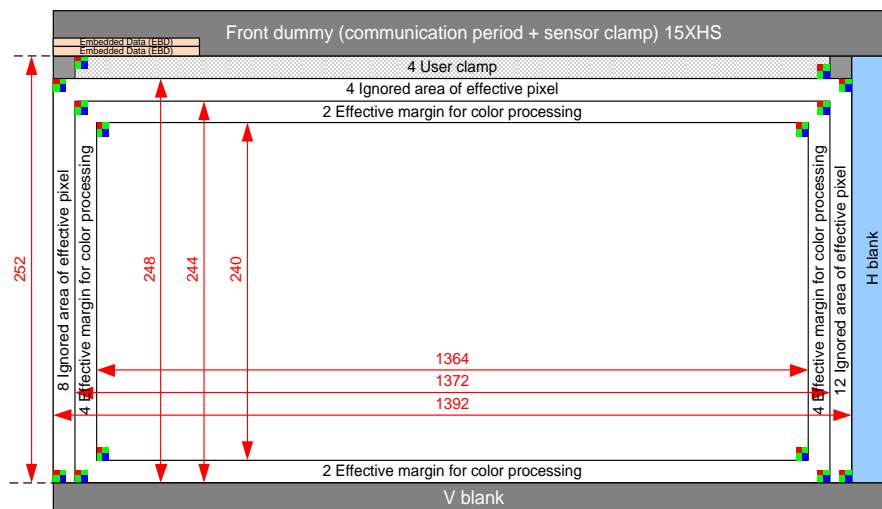


Readout Pixel Image Diagram (1364 x 720)

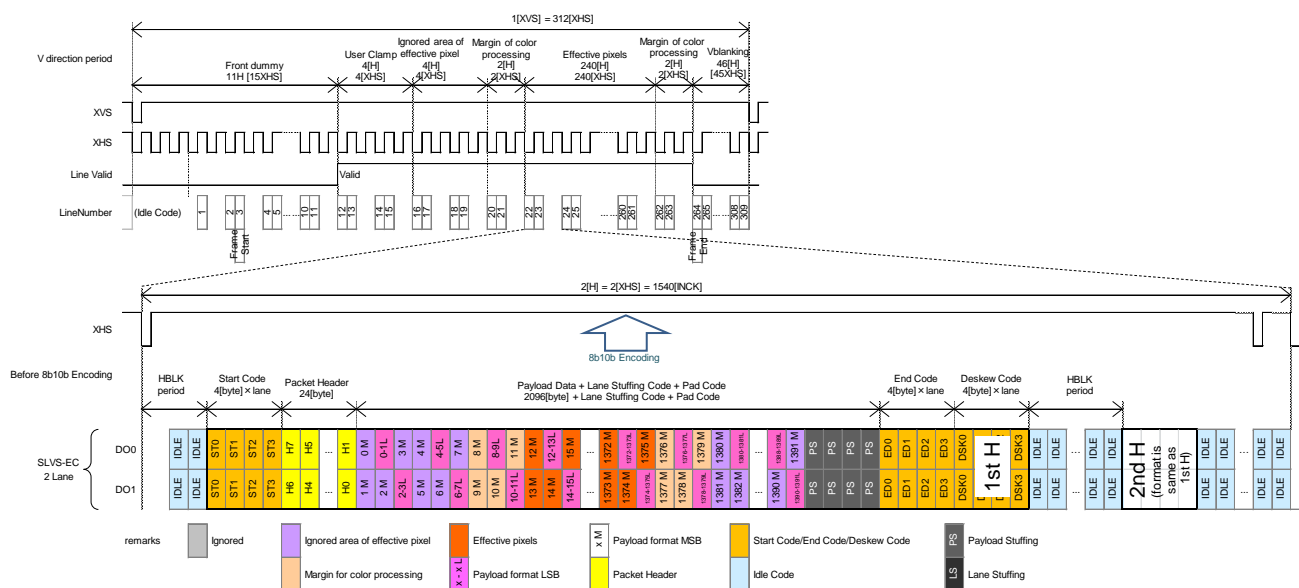


Readout Drive Timing

(SLVS-EC) MODE10: Vertical 2/9 subsampling binning horizontal 3 binning
(10-bit A/D conversion, 12-bit length output)

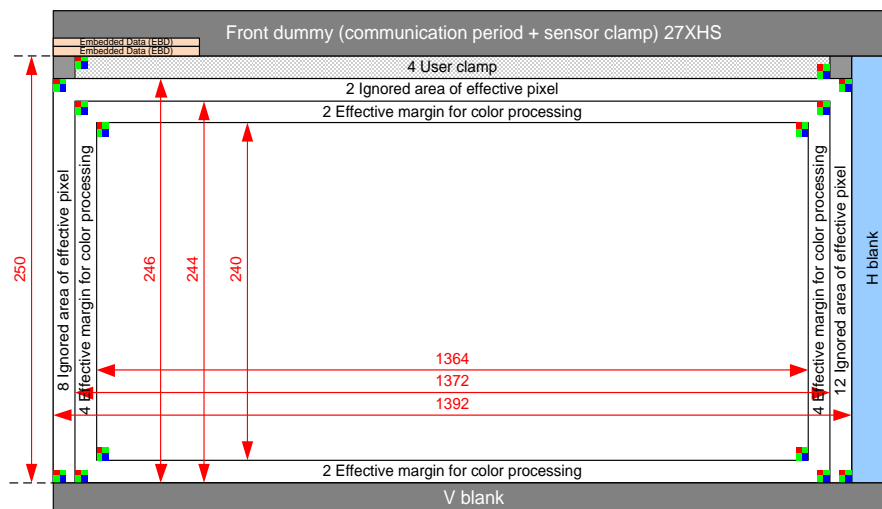


Readout Pixel Image Diagram (1364 x 240)

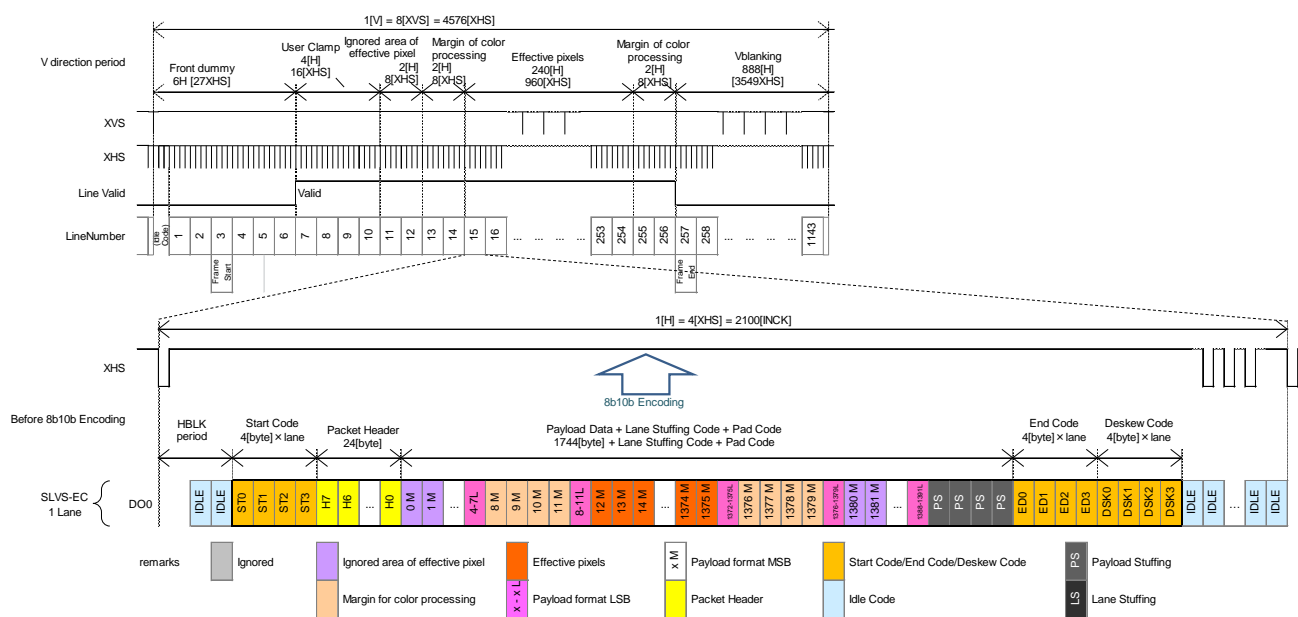


Readout Drive Timing

**(SLVS-EC) MODE11: Vertical 2/9 subsampling binning horizontal 3 binning low power consumption drive
(10-bit A/D conversion, 10-bit length output)**



Readout Pixel Image Diagram (1364 x 240)



Readout Drive Timing

2. When Using Aspect Ratio 4:3 (Approx. 10.71 M pixels)

2-1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (SLVS-EC)

Horizontal Operation Period in Each Readout Drive Mode (SLVS-EC)

Readout mode No.	Horizontal operation period (Number of pixels conversion)						XHS minimum period [INCK] ^{*1*2}	XHS number per H period
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel		
0	0	28	12	3704	12	36	1730	0.5
1	0	28	12	3704	12	36	706	0.5
1A	0	28	12	3704	12	36	1192	0.5
7	0	14	6	1852	6	18	520	0.5
10	0	10	4	1234	4	12	520	1

^{*1} Number of clocks in conversion of INCK = 72 MHz.

^{*2} If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.

Vertical Operation Period in Each Readout Drive Mode (SLVS-EC)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)							XVS minimum period [XHS]
	Vertical front blanking	Front OB (User Clamp)	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	24(15XHS)	16	8	18	2778	18	2	1435
1	24(15XHS)	16	8	18	2778	18	2	1435
1A	24(15XHS)	16	8	18	2778	18	2	1435
7	12(9XHS)	4	4	6	1388	6	0	713
10	11(15XHS)	4	4	2	308	2	0	335

2-2. Frame Rate Adjustment (SLVS-EC)

The formula for frame rate calculation is shown below.

$$\text{Frame rate [frame/s]} = (72 \times 10^6) / \{ \text{XHS period [INCK]} \times \text{XVS period [XHS]} \times (\text{SVR register value} + 1) \}$$

The frame rate can be changed by changing XHS period and XVS period as long as these are set to minimum value or larger. Larger XHS period results in longer horizontal blanking period. Larger XVS period results in longer vertical blanking period. The examples of setting for each readout drive mode are shown in the table below. Set XHS period and XVS period considering ISP image processing time.

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See "Electronic Shutter Timing" on page 133 for details.

Examples of XHS Period, XVS period and Frame Rate (SLVS-EC)

Readout mode No.	XHS min period (INCK) ^{*1}	XVS min period (number of XHS pulses)	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				XHS period (INCK) ^{*1}	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]	XHS period (INCK) ^{*1}	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]
0	1730	1435	29.00	1875	1600	0	24.00 ^{*2}	1800	1600	0	25.00
1	706	1435	71.07	715	1680	0	59.94	720	2000	0	50.00
1A	1192	1435	42.09	1232	1950	0	29.97	1250	2304	0	25.00
7	520	713	194.20	525	1144	0	119.88	576	1250	0	100.00
7 (60fps)				525	1144	1	59.94	576	1250	1	50.00
10	520	335	413.32	520	385	0	359.64	600	400	0	300.00
10 (30fps)				520	385	11	29.97	600	400	11	25.00

^{*1} Number of clocks in conversion of INCK = 72 MHz

^{*2} The frame rate is not compatible for NTSC.

2-3. Imaging Conditions in Each Readout Drive Mode (SLVS-EC)

Readout mode No.	Imaging conditions					
	Number of SLVS-EC output channels [lane]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	8	14	14	3704	2778	Approximately 10.29 M Pixels
1	8	12	12	3704	2778	Approximately 10.29 M Pixels
1A	6	12	12	3704	2778	Approximately 10.29 M Pixels
7	4	10	10	1852	1388	Approximately 2.57 M Pixels
10	4	10	12	1234	308	Approximately 0.38 M Pixels

(SLVS-EC) MODE0: All-pixel scan mode (14-bit A/D conversion, 14-bit length output)



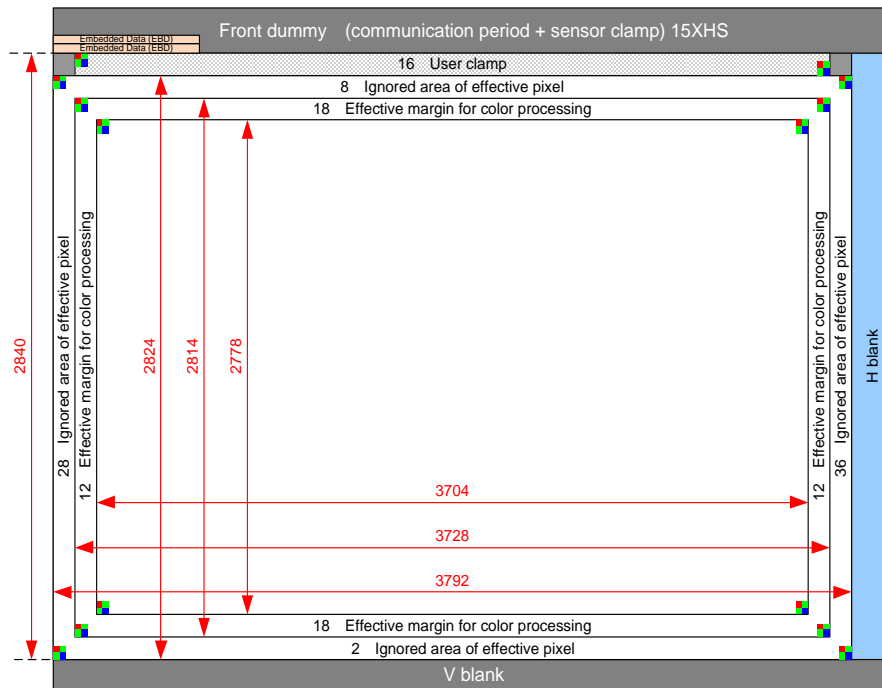
The diagram illustrates the 15XH5 sensor layout with the following dimensions and areas:

- Top Margins:**
 - 16 User clamp
 - 8 Ignored area of effective pixel
 - 18 Effective margin for color processing
- Left Margins:**
 - 28 Ignored area of effective pixel
 - 12 Effective margin for color processing
- Right Margins:**
 - 12 Effective margin for color processing
 - 36 Ignored area of effective pixel
- Bottom Margins:**
 - 18 Effective margin for color processing
 - 2 Ignored area of effective pixel
- Effective Areas (Horizontal):**
 - 3704
 - 3728
 - 3792
- Effective Areas (Vertical):**
 - 2824
 - 2814
 - 2778
- Overall Dimensions:**
 - 2840** (Total height)
 - V blank** (Total width)
- Other Labels:**
 - Embedded Data (EBD)
 - H blank

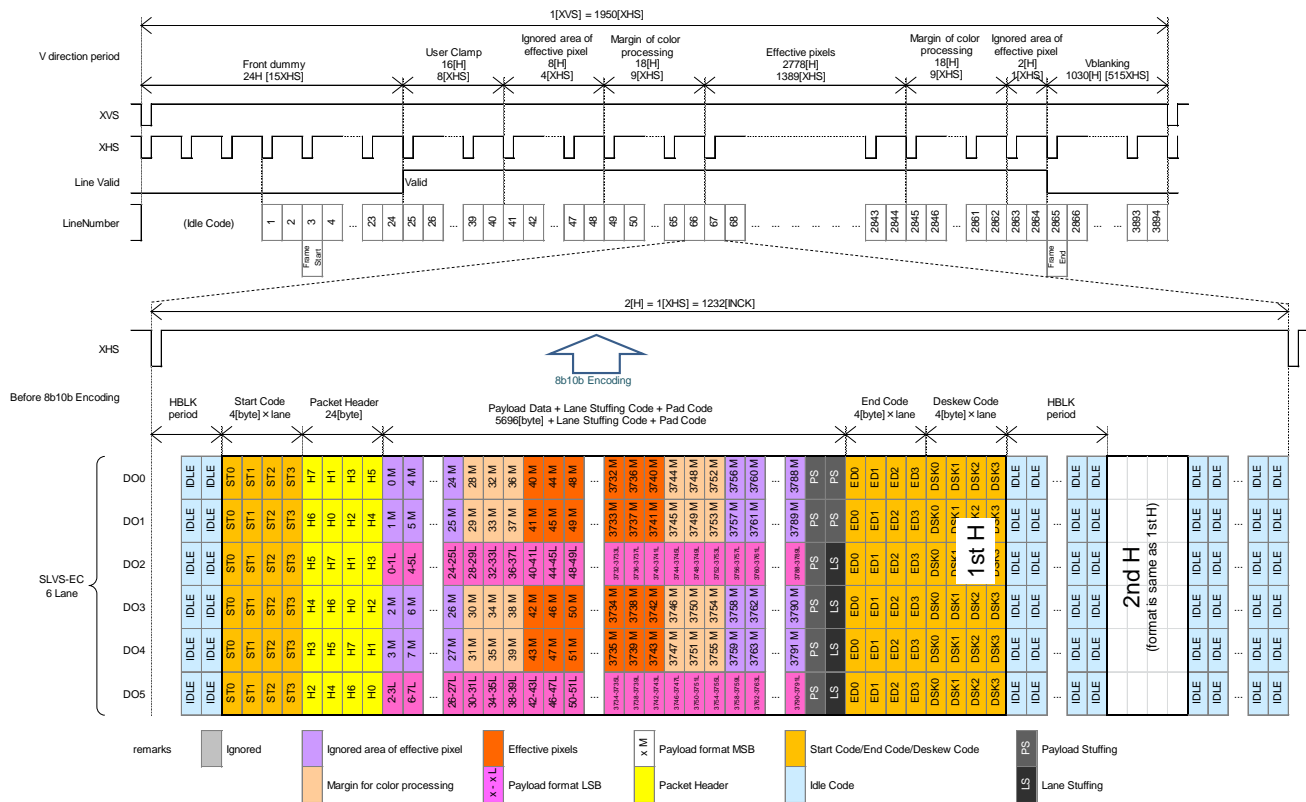
Readout Pixel Image Diagram (3704 x 2778)



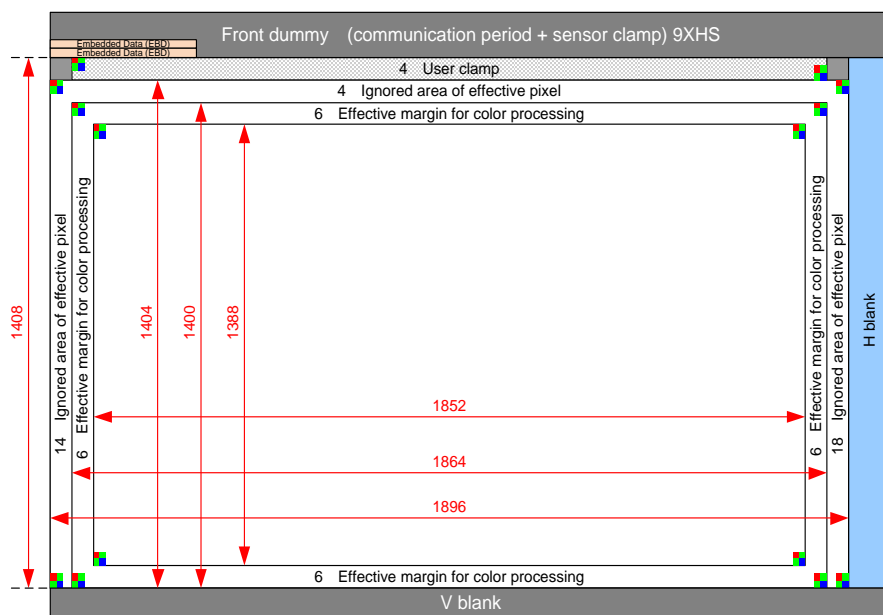
(SLVS-EC) MODE1A: All-pixel scan mode low noise
(12-bit A/D conversion, 12-bit length output)



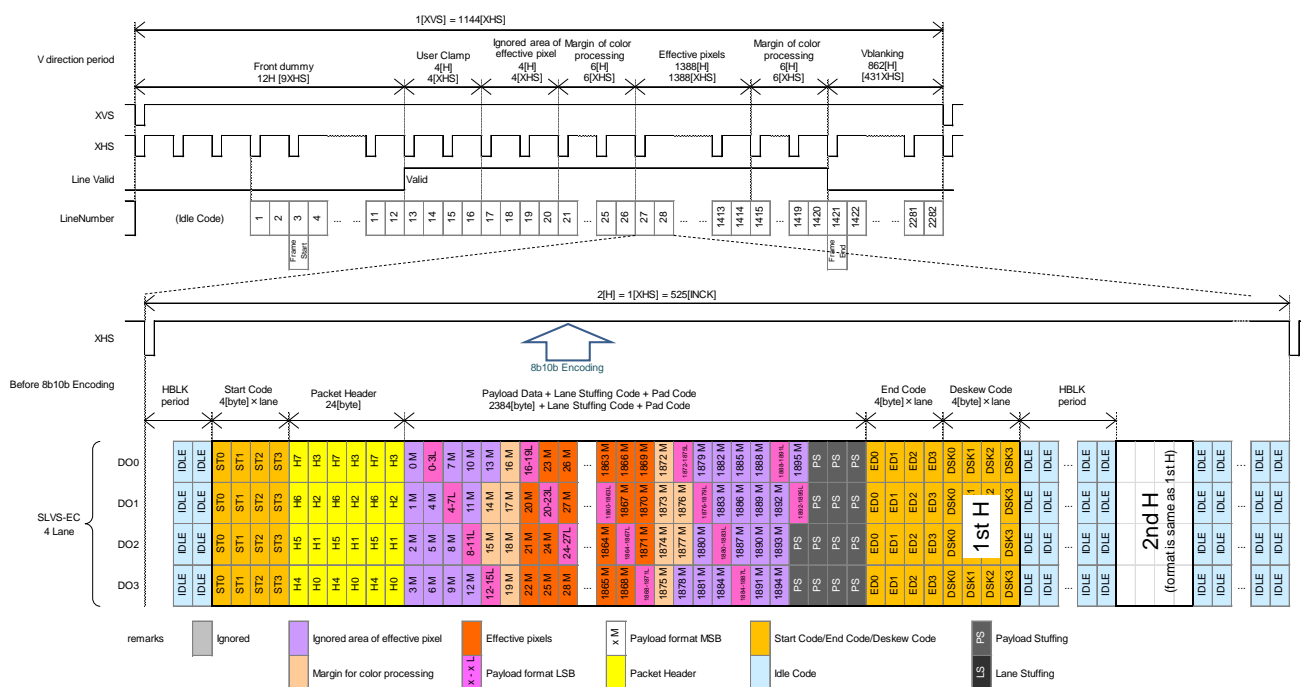
Readout Pixel Image Diagram (3704 × 2778)



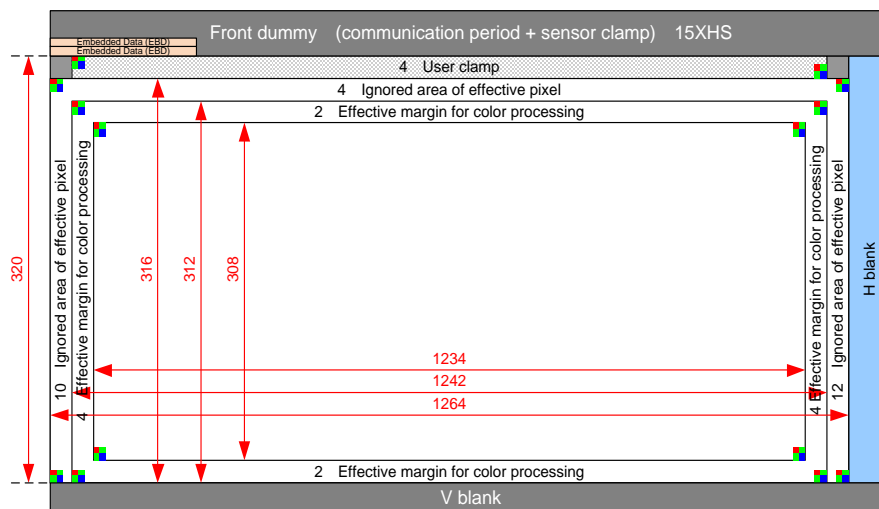
(SLVS-EC) MODE7: Horizontal/vertical 2/4 subsampling (10-bit A/D conversion, 10-bit length output)



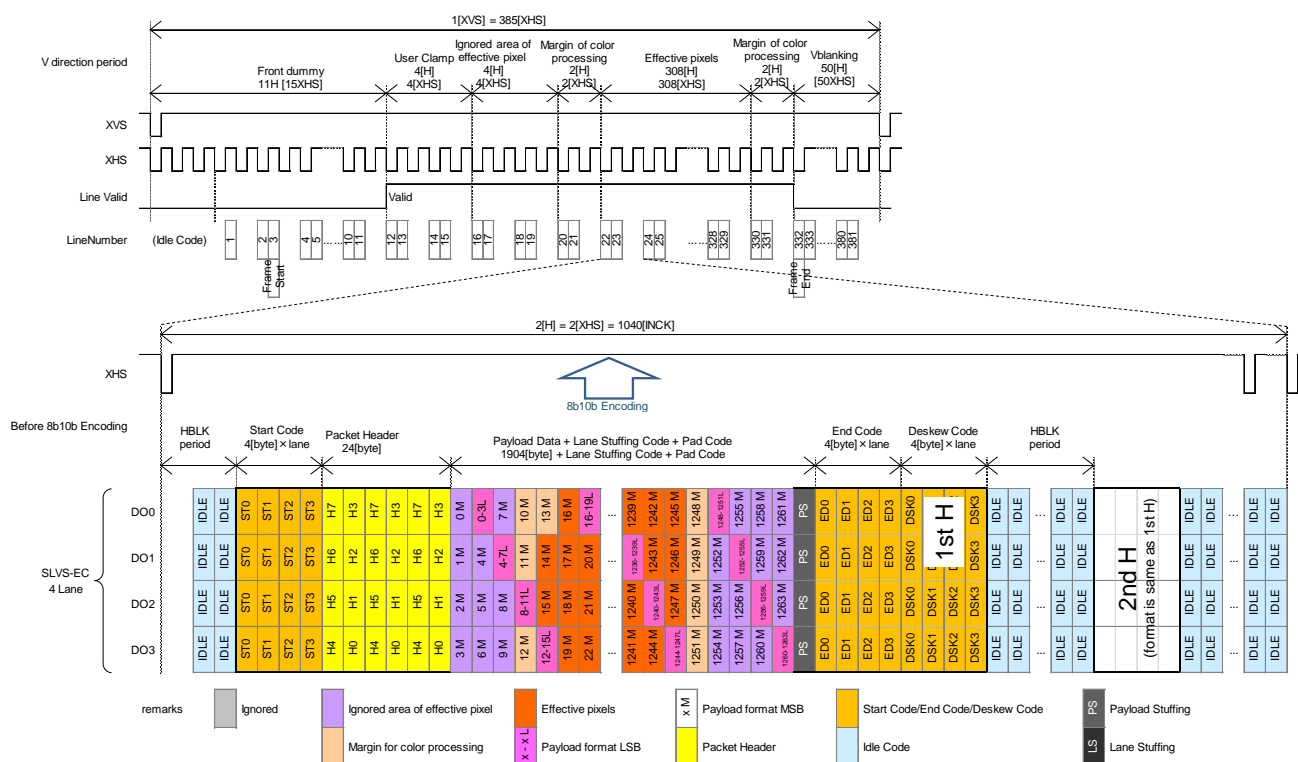
Readout Pixel Image Diagram (1852 × 1388)



(SLVS-EC) MODE10: Vertical 2/9 subsampling binning horizontal 3 binning
(10-bit A/D conversion, 12-bit length output)



Readout Pixel Image Diagram (1234 x 308)



Readout Drive Timing

Vertical Arbitrary Cropping (SLVS-EC)

Vertical cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings (SLVS-EC)

Enable vertical cropping with setting vertical arbitrary cropping enable register VWIDCUTEN to 1h, and specify cropping width by the vertical cropping width register VWIDCUT, and cropping position by the vertical cropping start position register VWINPOS.

Set VWINPOS negative value (two's complement) when the direction of vertical readout is inverted (MDVREV = 1h).

V_{eff} indicates the number of effective lines output before cropping (VWIDCUTEN = 0h) in following description.

VWIDCUTEN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function
VWIDCUTEN	—	00DDh	[0]	0h	Vertical arbitrary cropping is disabled
				1h	Vertical arbitrary cropping is enabled

VWIDCUT Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
VWIDCUT [7:0]	—	00DEh	[7:0]	Specify vertical cropping width
VWIDCUT [13:8]	—	00DFh	[5:0]	Output height [line] = $V_{eff} - VWIDCUT \times \text{step}$

VWINPOS Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value
VWINPOS [7:0]	—	00E0h	[7:0]	Vertical cropping start position (two's complement)
VWINPOS [13:8]	—	00E1h	[5:0]	New start position (in output image) [line] = $VWINPOS \times \text{step}$

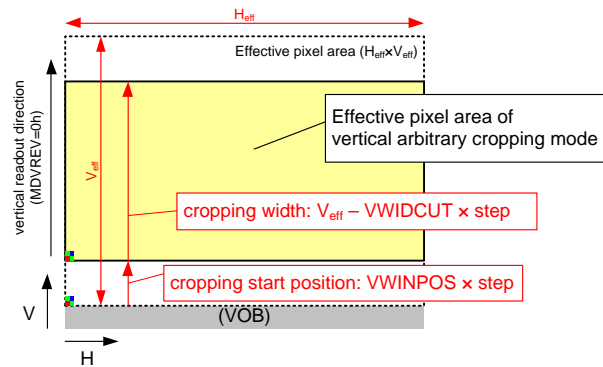
Refer to the following table in the value of step.

Vertical Arbitrary Cropping Step

Readout mode No.	step value
4, 6, 11	2
0, 1, 1A, 1B, 2, 2A, 3, 5, 7, 8, 9, 10	4

When vertical readout direction is normal (MDVREV = 0h), relation between register setting values of VWINPOS / VWIDCUT and cropping region on physical pixel array is shown below.
Register setting values must satisfy following relations. (Setting ranges are within those values which satisfy following.)

- VWINPOS × step ≥ 0 (Starting position of readout must be 0 or more)
- $V_{\text{eff}} - \text{VWIDCUT} \times \text{step} \geq V_{\text{eff}} / 2$ (Number of readout lines must be 1/2 or more before cropping)
- $\text{VWINPOS} \times \text{step} + V_{\text{eff}} - \text{VWIDCUT} \times \text{step} \leq V_{\text{eff}}$ (End position of readout must be within the area before cropping)



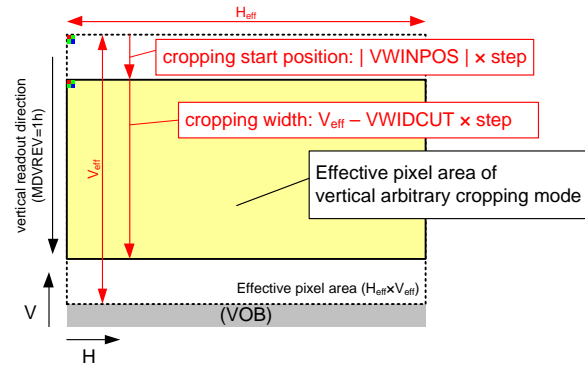
Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array
(Vertical Readout Direction Normal)

For example, when the top 400 lines and bottom 400 lines (totally 800 lines) of mode No.1 of aspect ratio approx. 17:9 all-pixel scan area (approx. 9.07M pixels), all-pixel scan area is skipped and start cropping readout from the 401st line, setting values are as follows:

VWIDCUT 00C8h (200d) / VWINPOS 064h (100d) (step = 4 for mode1)

When vertical readout direction is inverted (MDVREV = 1h), relation between register setting value of VWINPOS / VWIDCUT and cropping region is shown below. Register setting values must satisfy following relations also. Note that VWINPOS must be negative.

$|VWINPOS| \times \text{step} \geq 0$ (Starting position of readout must be 0 or more)
 $V_{\text{eff}} - VWIDCUT \times \text{step} \geq V_{\text{eff}} / 2$ (Number of readout lines must be 1/2 or more before cropping)
 $|VWINPOS| \times \text{step} + V_{\text{eff}} - VWIDCUT \times \text{step} \leq V_{\text{eff}}$ (End position of readout must be within the area before cropping)



Relation between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array (Vertical Readout Direction Inverted)

For example, when the top 400 lines and bottom 400 lines (total 800 lines) of mode1 all-pixel scan area (when vertical readout direction inverted) is skipped and start cropping readout from the 401st line, setting values are as follows:

VWIDCUT 00C8h (200d) / VWINPOS F9Ch (-100d) (step = 4 for mode1)

(2) Vertical Minimum Period When Using Vertical Arbitrary Cropping Function (SLVS-EC)

When using vertical arbitrary cropping function, XVS minimum period gets smaller according to cropping width. XVS minimum period after cropping follows the formula below using V_{MAX0} (XVS minimum period before cropping).

XVS minimum period = $V_{\text{MAX0}} - VWIDCUT \times \text{step} \times \text{XHS number per H period}$

For example, when using readout mode No.1 of aspect ratio approx. 17:9 all-pixel scan area (approx. 9.07M pixels), if you use cropping of VWIDCUT=00C8h(=200d), VMAX minimum value is $1107 - 200 \times 4 \times 0.5 = 707$. ($V_{\text{MAX0}} = 1107$ and XHS number per H period is 0.5)

Horizontal arbitrary cropping function (SLVS-EC)

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

(1) Register Settings (SLVS-EC)

Set horizontal cropping enable register HTRIMMING_EN to 1h to enable horizontal arbitrary cropping function, and horizontal cropping area are determined by horizontal cropping position register HTRIMMING_START and HTRIMMING_END.

HTRIMMING_EN Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Function	Remarks
HTRIMMING_EN	—	0035h	[0]	0h	Horizontal arbitrary cropping OFF	Send with register setting for each readout drive mode.
				1h	Horizontal arbitrary cropping ON	

Horizontal Arbitrary Cropping Position Setting

Name	CSI-2 (I ² C) Address	SLVS-EC Address	Bit	Register value	Remarks
HTRIMMING_START [7:0]	—	0036h	[7:0]	horizontal cropping start position ^{*1}	Unit: pixel Send with register setting for each readout drive mode.
HTRIMMING_START [13:8]	—	0037h	[5:0]		
HTRIMMING_END [7:0]	—	0038h	[7:0]	horizontal cropping end position ^{*1} + 1	
HTRIMMING_END [13:8]	—	0039h	[5:0]		

^{*1} In the readout mode with horizontal binning or subsampling, set the value of HTRIMMING_START and HTRIMMING_END according to the position before processing horizontal binning or subsampling.

HTRIMMING_START and HTRIMMING_END must satisfy following 3 restrictions.

$$\begin{aligned} \text{HTRIMMING_START} &= 48 + N \times \text{step1} \\ \text{HTRIMMING_END} &= \text{HNUM} - M \times \text{step2} \\ \text{HTRIMMING_END} - \text{HTRIMMING_START} &\geq \text{Minimum value} \\ (\text{M and N are integers equal or more than 0}) \end{aligned}$$

Refer to the following tables in the value of step1, step2, HNUM and Minimum value.

Step value

Readout mode Horizontal pixel processing	no binning	Horizontal 2 binning	Horizontal 3 binning	Horizontal 2/4 subsampling
step1	12	12	12	24
step2	4	24	12	24

Minimum value of HTRIMMING_END – HTRIMMING_START

Readout mode Horizontal pixel processing	no binning	Horizontal 2 binning	Horizontal 3 binning	Horizontal 2/4 subsampling
Minimum value	36	72	96	72

HNUM value

Readout mode No.	When Using Aspect Ratio Approx. 17:9 (Approx. 9.07M pixels)		When Using Aspect Ratio 3:2 (Approx. 10.71M pixels)
	1, 2	1A, 2A, 3, 4, 5, 6, 7, 8, 9, 10, 11	0, 1, 1A, 7, 10
HNUM	4192	4224	3840

(2) Horizontal Minimum Period When Using Horizontal Arbitrary Cropping Function (SLVS-EC)

When using horizontal arbitrary cropping function, XHS minimum period is as follows:

XHS Minimum Period When Using Horizontal Arbitrary Cropping Function

Readout mode No.	XHS minimum period [INCK]
0	1730
1	$\max(706, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 1/6 + 34.0)$
1A	1192
2	520
2A	827
3	706
4	706
5	520
6	520
7	520
8	520
9	520
10	$\max(520, [\text{HTRIMMING_END} - \text{HTRIMMING_START}] \times 1/6 + 46.0)$
11	520

* $\max(A, B)$ means the larger value of A and B.

* Fractions should be rounded up.

Electronic Shutter Timing When Using SLVS-EC

1. SHR, SVR Setting (SLVS-EC)

The exposure start timing can be designated by setting the electronic shutter timing register SHR.

Note that this setting value unit is 1XHS period regardless of the readout drive mode. In addition, the vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal period inside is (SVR value + 1) times as long as XVS signal period.

Shutter Setting (SLVS-EC)

Name	SLVS-EC Address	Bit	Function
SHR [7:0]	002Ch	[7:0]	Specifies the integration start horizontal period
SHR [15:8]	002Dh	[7:0]	
SVR [7:0]	000Eh	[7:0]	Specifies the integration shutdown vertical period
SVR [15:8]	000Fh	[7:0]	

Shutter Control Register Setting Range (SLVS-EC)

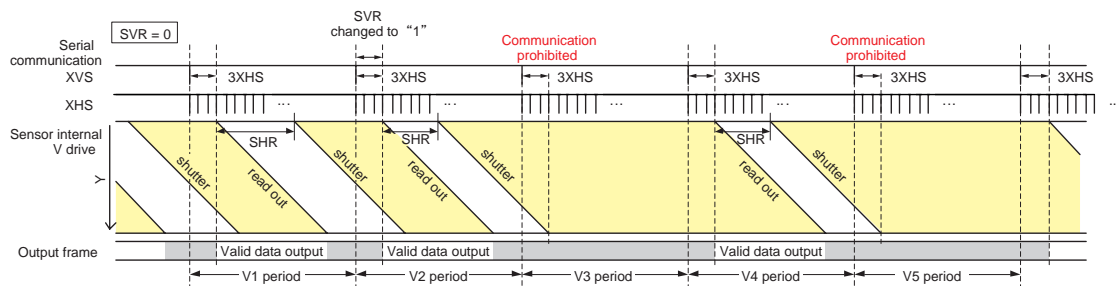
Register	Register Value		Function
SHR	5 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No.0, 1, 1A, 2, 2A All-pixel scan mode (14 bits, 12 bits, 10 bits) All-pixel scan mode (12 bits) low noise All-pixel scan mode (10 bits) low noise	Specifies the integration start horizontal period
	5 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No.3, 5 Horizontal/vertical 2/2-line binning mode (Horizontal and vertical weighted binning)	
	3 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No.4 Horizontal/vertical 2/2-line binning mode (Horizontal and vertical weighted binning)	
	5 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No. 6 Vertical 2 binning horizontal 2/4 subsampling (Vertical weighted binning)	
	3 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No. 7 Horizontal/vertical 2/4 subsampling	
	7 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No.8, Horizontal/vertical 3/3 binning	
	2 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No.9 Vertical 1/3 subsampling Horizontal 3 binning	
	5 to {(SVR value + 1) × Number of XHS pulses per frame - 1}	Readout mode No. 10 Vertical 2/9 subsampling binning Horizontal 3 binning	
	5 to {(SVR value + 1) × Number of XHS pulses per frame / 4 - 1}	Readout mode No. 11 Vertical 2/9 subsampling binning Horizontal 3 binning low power consumption	
	1 to {(SVR value + 1) × Number of XHS pulses per frame - 43}	Global reset shutter mode (SMD = 1)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

Note)

1. See "Integration Time in Each Readout Drive Mode" on page 135 for the integration time calculation formula.
2. The SVR setting range is guaranteed as sensor functions, characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 0008h, bit [0]).

2. SVR Operation (SLVS-EC)

Example of Electronic Shutter Operation when using SLVS-EC is shown below.



Example of SVR operation

Note) In vertical sync signal subsampling periods (Example of SVR Operation: V3 and V5 periods), communication is prohibited during the normal communication period (the 3XHS period after the vertical sync signal XVS is input), except in the following case.

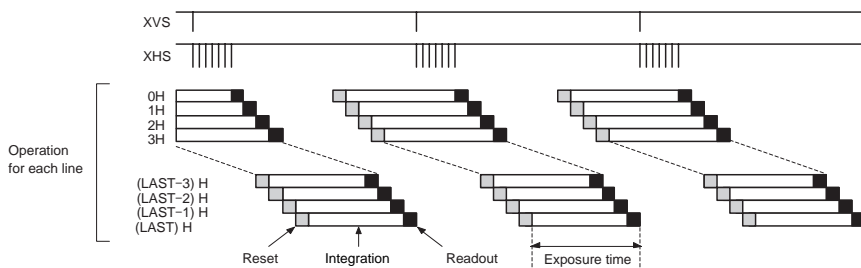
* When stopping vertical sync signal subsampling using the break mode register SSBK.

3. Electronic Shutter Drive Mode (SLVS-EC)

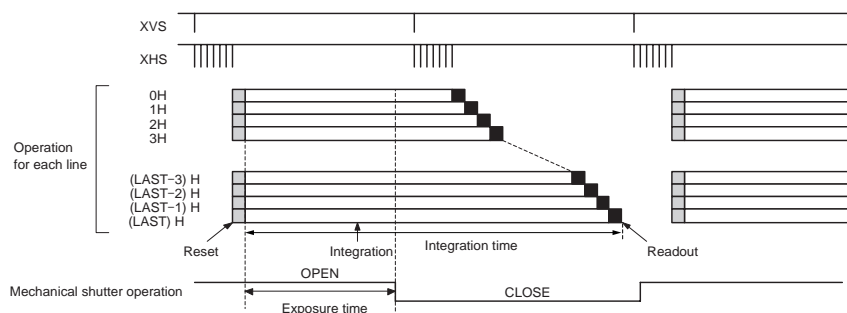
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD. Rolling shutter operation performs pixel reset and integration sequentially in line units in sync with the XHS signal. Global reset shutter operation resets all pixels at once and then starts integration after that. ("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.) The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.

SMD Setting

Name	SLVS-EC Address	Bit	Register value	Function
SMD	0008h	[0]	0h	Rolling shutter (normal shutter mode)
			1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

4. Integration Time in Each Readout Drive Mode and Mode Changes When Using SLVS-EC

4-1. Integration Time in Each Readout Drive Mode (SLVS-EC)

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR, SVR and SPL. The formulas and constants used to calculate the integration time are shown below. In addition, the frame rate can be reduced by setting the SVR register to "1" or more.

◆ Integration time of normal readout drive mode (other than mode No.11)

$$\text{Integration Time [s]} = \left[\{ \text{Number of XHS per XVS period} \times (\text{SVR value} + 1) - (\text{SHR value}) \} \times \text{Number of clock per XHS Period} + \text{Number of clocks per internal offset period} \right] / \text{INCK frequency [Hz]}$$

* See the following tables for the numbers of clocks per internal offset period.

* See "Electronic Shutter Timing" on page 133 for the SHR register setting range.

◆ Integration time of normal readout drive mode No.11

$$\text{Integration Time [s]} = \left[\{ \text{Number of XHS per XVS period} \times (\text{SVR value} + 1) - (\text{SHR value}) \times 4 \} \times \text{Number of clock per XHS Period} + \text{Number of clocks per internal offset period} \right] / \text{INCK frequency [Hz]}$$

* See the following tables for the numbers of clocks per internal offset period.

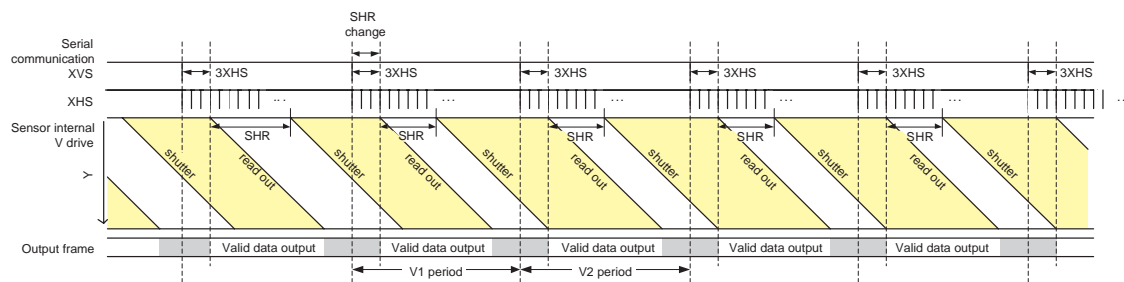
* See "Electronic Shutter Timing" on page 133 for the SHR register setting range.

Number of clocks per internal offset period (SLVS-EC)

Readout mode No.	0	1	1A	2	2A	3	4	5	6	7	8	9	10	11
Number of clocks per internal offset period	551	256	361	217	322	256	256	217	217	217	217	217	217	217

The figure below shows operation when changing SHR.

The V1 and V2 periods in the figure below are two continuous XVS periods. The SHR value set within the first 3XHS periods (recommended serial communication period) of V1 is updated internally at the end of the 3XHS periods, and then output data which reflect the new setting is output in the V2 period. Note that the SHR setting and output are offset by 1XVS period.

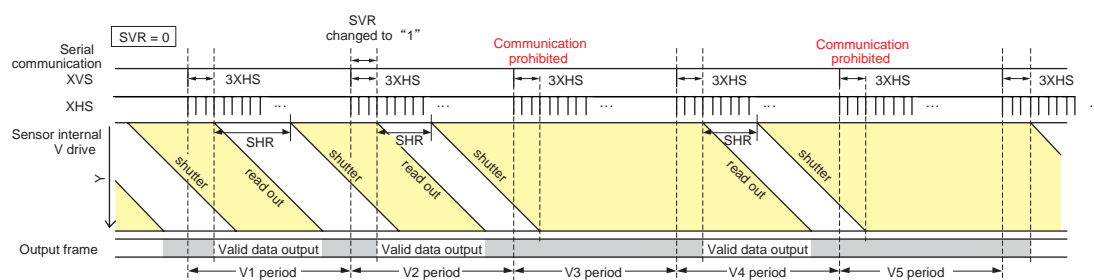


SHR Change Sequence (SLVS-EC)

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal period inside the sensor is (SVR value + 1) times as long as XVS signal period. Therefore the frame rate is multiplied by $1/(SVR \text{ value} + 1)$ according to the SVR value.

The figure below shows the operation when changing the SVR register. The example in the figure below shows the update timing when the SVR value is changed from "0" to "1". The SVR value set within the first 3XHS periods (recommended serial communication period) of V2 is updated internally at the end of the 3XHS periods, and then applied from the shutter operation in the V2 period. Readout operation is not performed in the V3 period, and output data which reflect the changing of SVR is output in the V4 period.

The image data of the V1 period before the SVR value is changed is output as valid data in the V2 period. In addition, note that communication is also prohibited during the first 3XHS periods (recommended serial communication period) of the V3 period (the frame during which readout operation is not performed)



SVR Change Sequence (SLVS-EC)

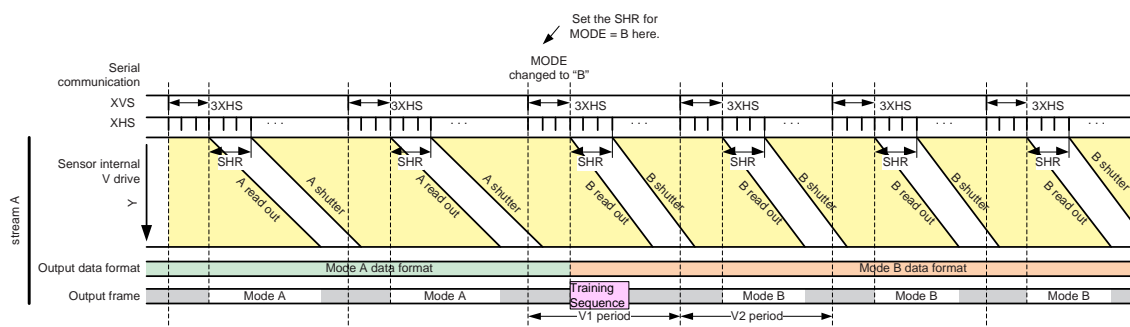
4-2. Operation when Changing the Readout Drive Mode (SLVS-EC)

The following change cases are treated as mode transition on this sensor.

1. Changing the readout mode setting
2. Changing the vertical direction readout inversion setting
3. Changing the vertical arbitrary cropping setting
4. Changing the horizontal arbitrary cropping setting

A training sequence is generated automatically from 1 to 3. In 4 a training sequence must be generated by manually set MDCHGRST to 1. In both cases effective data output stops for 1 frame.

The figure below shows the mode transition sequence (Mode A to Mode B). The output of the frame changed to Mode B (V1 period) is the training sequence of Mode B. Valid data is output from the next frame (V2 period). If XHS period varies between Mode A and Mode B, set XHS period in the timing shown in the figure below (head of V1 period)



Mode Transition (SLVS-EC)

4-3. Recommended Global Reset Shutter Operation Sequence (SLVS-EC)

The recommended global reset shutter operation sequence is shown below. Operation in this mode spans plural XVS periods. Global reset shutter is performed in the first XVS period, and the data is output in following other XVS periods.

The exposure time can be adjusted by varying the XVS input period. However, the minimum XVS period is 15 XHS periods. In addition, the mechanical shutter must also be used to make the exposure time the same for all pixels. See "Electronic Shutter Timing" on page 133 for the SHR register setting range.

Recommended Operating Sequence for Global Reset Shutter (SLVS-EC)

Operation item	Description	Explanatory diagram
Normal	When performing global reset shutter partway through rolling shutter operation	Global reset shutter normal operation
Continuous	When performing global reset shutter operation continuously	Global reset shutter continuous operation

Normal Operation (SLVS-EC)

Operation when performing global reset shutter + all-pixel scan (12 bits) one time partway through rolling shutter operation is shown below.

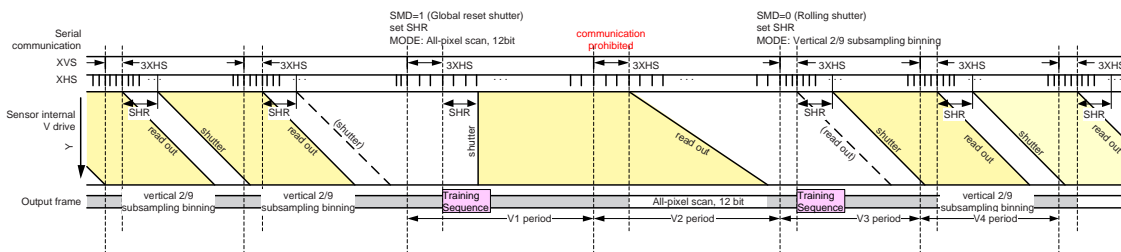
Vertical 2/9 subsampling binning horizontal 3 binning mode is described as a typical example of rolling shutter operation, but the transition operation is the same for all modes that use rolling shutter.

V1 to V4 in the figure below are the four continuous XVS periods. When the global reset shutter settings (SMD = 1h, register setting for all-pixel scan mode (12 bits)) are made within the first 3XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the 3XHS period. Global reset shutter readout data is output during the V2 period.

Communication to return to the original mode (SMD = 0h, register setting for vertical 2/9 subsampling binning horizontal 3 binning, SHR should also be changed as necessary) is performed at the start of the V3 period.

The output data for the frame immediately after that (the V3 period in the figure) are invalid.

Note that communication is also prohibited during the first 3XHS periods (recommended serial communication period) of the V2 period. The two tables below shows the possible length of XVS period in integration frame (V1) and the integration start time in the exposure start XVS period (V1).



Global Reset Shutter Normal Operation (SLVS-EC)

Possible Length of XVS period in Integration Frame of Global Reset Shutter (SLVS-EC)

Condition	Possible Length of XVS period in Integration Frame
Without the training sequence	≥ 15 XHS periods
With the training sequence	≥ 3 XHS periods + 43000 [INCK] ^{*1*2} and ≥ 15 XHS periods

^{*1} Number of clocks in conversion of INCK = 72 MHz

^{*2} When SLVS-EC parameters are default.

Integration Start Time of the Exposure Start Period (SLVS-EC)

Readout mode No.	Integration start time of the exposure start period (XVS reference)
0	Approx. 417 [INCK] after the (3 + SHR) XHS period ends ^{*1}
1, 1A, 3, 4	Approx. 351 [INCK] after the (3 + SHR) XHS period ends ^{*1}
2, 2A, 5 to 11	Approx. 337 [INCK] after the (3 + SHR) XHS period ends ^{*1}

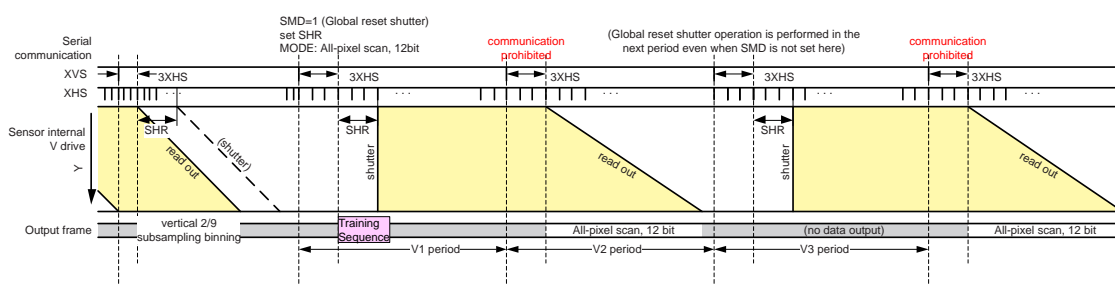
^{*1} Number of clocks in conversion of INCK = 72 MHz

Continuous Operation (SLVS-EC)

Operation when continuously performing global reset shutter + all-pixel scan (12 bits) is shown below. V1 to V3 in the figure below are three continuous XVS periods. When the global reset shutter + all-pixel scan (12 bits) settings (SMD = 1h, register setting for all-pixel scan mode (12 bits)) are made within the first 3XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the first 3XHS period of the V1 period. The training sequence is output in V1 period, and the all-pixel scan (12 bits) data is output in the V2 period. Note that communication is also prohibited during the first 3XHS periods (recommended serial communication period) in the V2 period.

The operation during V1 and V2 periods is then repeated each time XVS is input until the mode setting is changed next. However the training sequence is not output from the second time.

See the previous section for a description of the procedure when changing from continuous operation to a different readout mode.



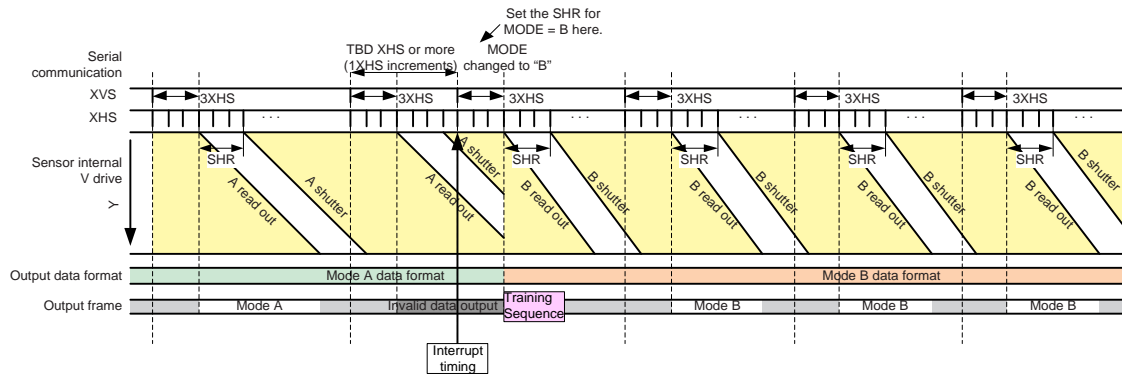
Global Reset Shutter Continuous Operation (SLVS-EC)

4-4. Interruptive Mode Change (SLVS-EC)

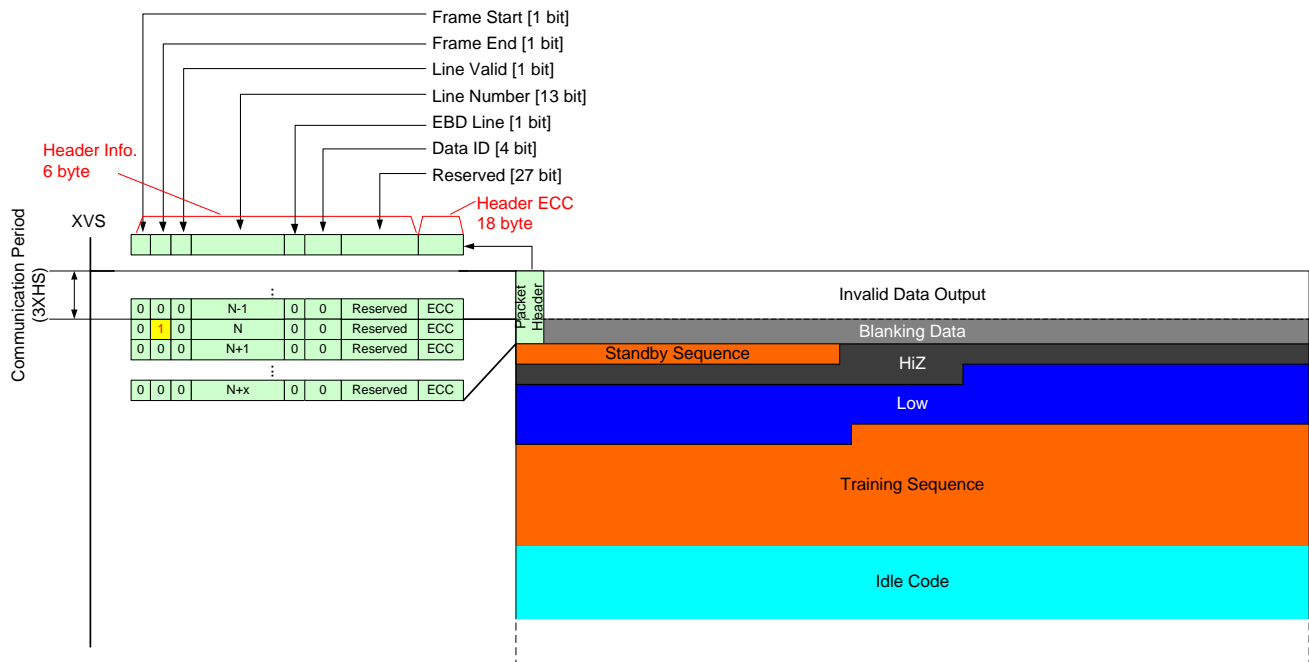
The sensor mode can be changed using interrupts in all modes.

When changing the mode using an interrupt, the mode can be changed by inputting XVS in sync with XHS after 15 XHS periods or more^{*1} have elapsed from the start of the frame, and transmitting the mode setting register value within the communication period. In addition, the data output before the interrupt mode change is cut off at the timing of the interrupt mode change. This case is shown in the figure below: "Frame Format of Interruptive Mode Change". Frame End = 1 is output at the 4th XHS period, and after that training sequence starts.

^{*1} When the mode before the change (Mode A in the figure below) is readout mode No.11 (low power consumption drive), wait 51 XHS periods or more from the start of the frame.



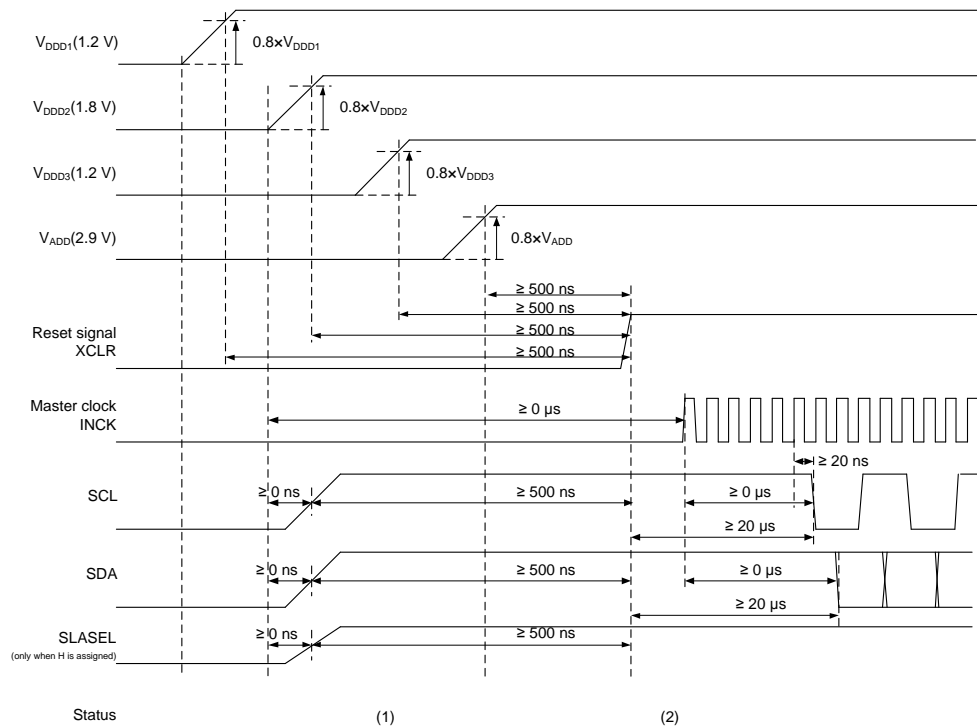
Interruptive Mode Change (SLVS-EC)



Frame Format of Interruptive Mode Change
(With Cutting Off of Previous Line Data)

Power-on/off Sequence when using CSI-2

1. Power-on Sequence (CSI-2)

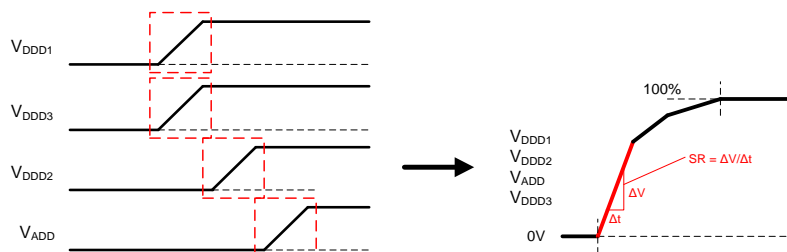


Power-on Sequence (CSI-2)

Period name	Remarks
(1) Power stabilization period	All input signals are set to Low level. There are no constraints of the power-on sequence with V_{ADD} , V_{DD1} , V_{DD2} and V_{DD3} .
(2) Register communication period for standby cancel	Wait 500 ns after the last power supply in V_{ADD} , V_{DD1} , V_{DD2} and V_{DD3} . Then set XCLR to "H" and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence (CSI-2)

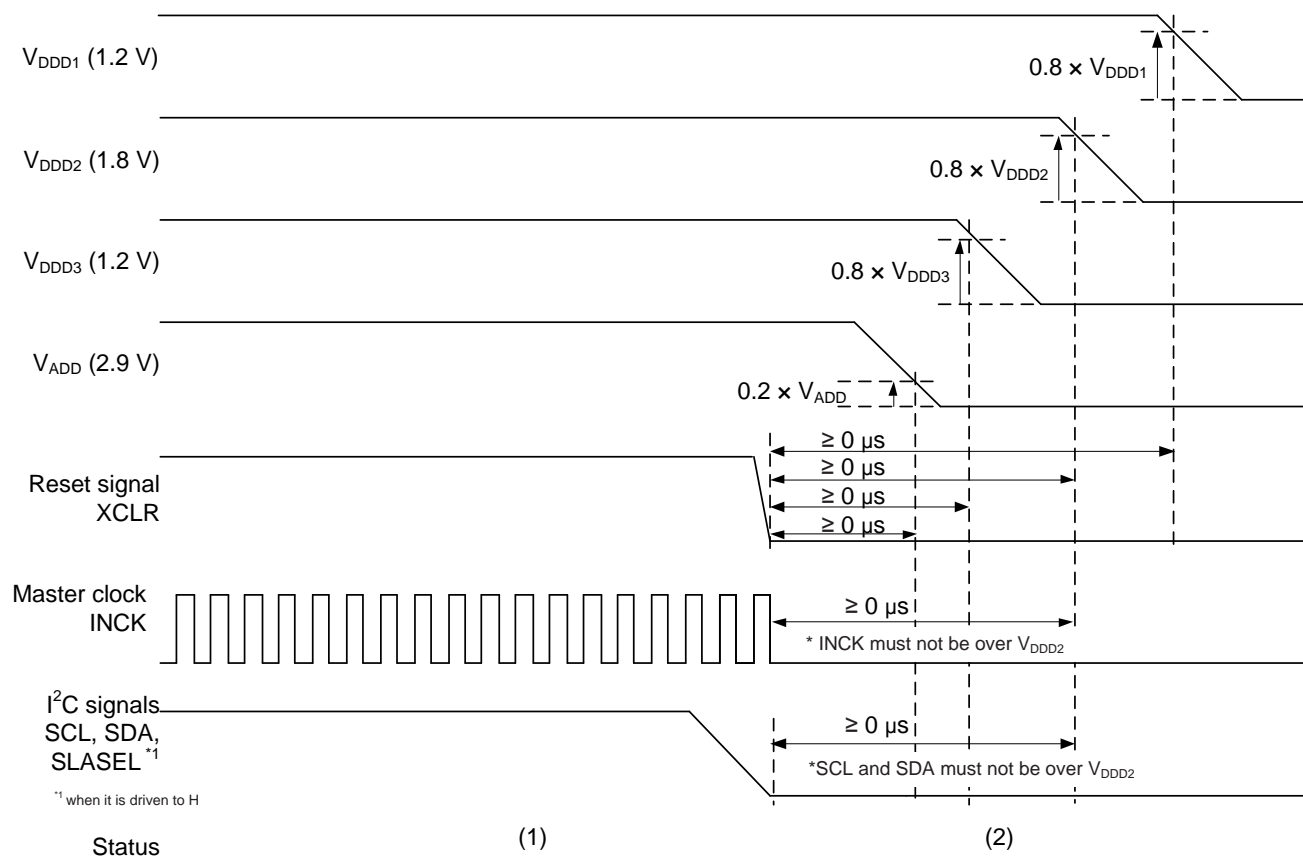
Conform to the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DD1} (1.2 V)	—	25	mV/us	
		V_{DD2} (1.8 V)	—	25	mV/us	
		V_{DD3} (1.2 V)	—	25	mV/us	
		V_{ADD} (2.9 V)	—	25	mV/us	

3. Power-off Sequence (CSI-2)

Make sure that all input signals are set to LOW level in the area of (2).



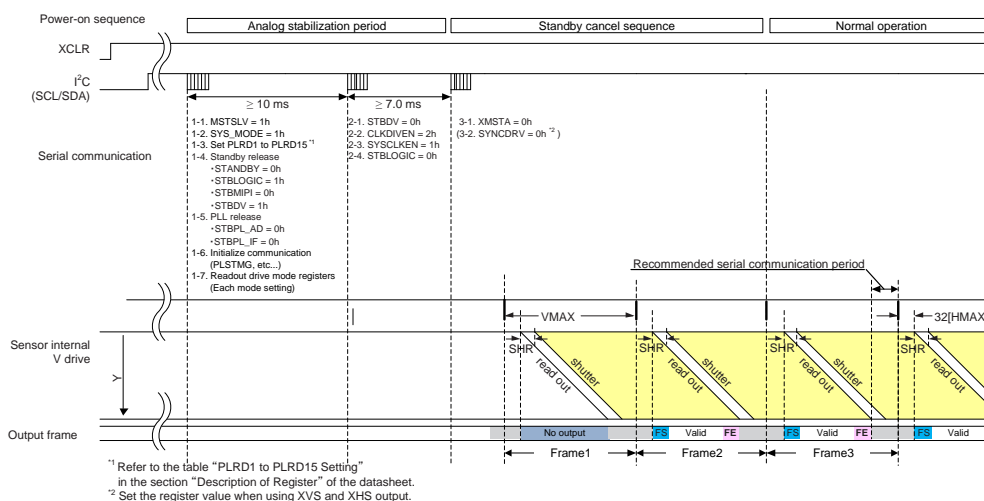
Power-off Sequence (CSI-2)

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	<p>Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA.</p> <p>Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DD2}.</p> <p>There are no constraints of the power-off sequence with V_{ADD}, V_{DD1}, V_{DD2} and V_{DD3}.</p>

Standby Cancel Sequence when using CSI-2

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancels sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

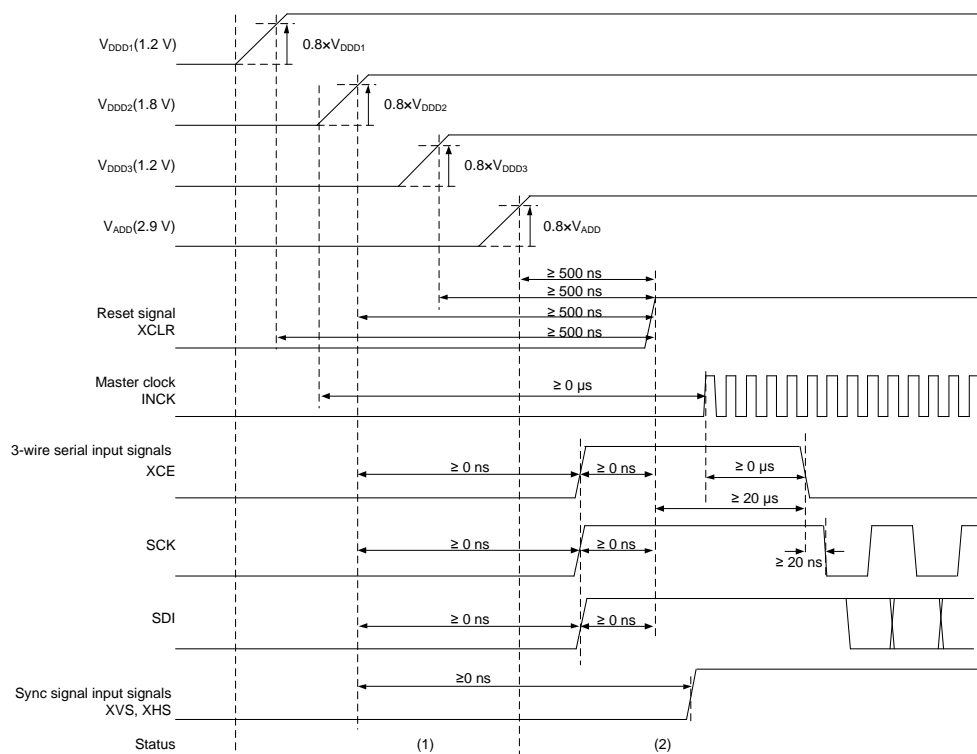
1. After performing the power-on start-up sequence, make the following register setting.
 - 1-1. Set address 3033h to 30h (XMSTA register = 1h, MSTSLV register = 1h)
 - 1-2. Set address 303Ch to 1h (SYS_MODE register = 1h)
 - 1-3. PLL Setting
 - Set the following registers to the appropriate value according to INCK's frequency.
 - Refer to "Description of Register" of "Register Map" on page 50.
 - Address 31E8h, bit[7:0] and Address 31E9h, [7:0] (PLRD1 register)
 - Address 3122h, bit[7:0] (PLRD2 register), Address 3129h, bit[7:0] (PLRD3 register)
 - Address 312Ah, bit[7:0] (PLRD4 register), Address 311Fh, bit[7:0] (PLRD10 register)
 - Address 3123h, bit[7:0] (PLRD11 register), Address 3124h, bit[7:0] (PLRD12 register)
 - Address 3125h, bit[7:0] (PLRD13 register), Address 3127h, bit[7:0] (PLRD14 register)
 - Address 312Dh, bit[7:0] (PLRD15 register)
 - 1-4. Standby Cancel
 - Set address 3000h to 12h (STANDBY register = 0h, STBLOGIC register = 1h, STBMPPI register = 0h, STBDV register = 1h).
 - 1-5. PLL release
 - Set address 310Bh to 00h (STBPL_IF register = 0h, STBPL_AD register = 0h).
 - 1-6. Initialize communication
 - 1) Set all registers of PLSTMG settings. (See "Readout Drive Pulse Timing" on page 55)
 - 2) Set all of Global Timing Registers. (See page 56)
 - Register communication can be performed even when STANDBY is 1h and there is no restriction on the communication order.
 - 1-7. Set Readout drive mode registers
 - Set the mode registers of the "Register Setting for Each Readout Drive Mode" on pages 62, 63 and 66.
 - Furthermore, set the required shutter and gain registers.
2. After the 1st stabilization period of 10 ms or more, make the following register setting.
 - 2-1. Set address 3000h to 02h (STANDBY register = 0h, STBLOGIC register = 1h, STBMPPI register = 0h, STBDV register = 0h).
 - 2-2. Set address 35E5h to 92h (CLKDIVEN register = 2h, SYSCLKEN register = 0h)
 - 2-3. Set address 35E5h to 9Ah (CLKDIVEN register = 2h, SYSCLKEN register = 1h)
 - 2-4. Set address 3000h to 00h (STANDBY register = 0h, STBLOGIC register = 0h, STBMPPI register = 0h, STBDV register = 0h).
3. After the 2nd stabilization period of 7.0ms or more,
 - 3-1. Set address 3033h to 20h (XMSTA register = 0h).
 - 3-2. Set address 3017h to A8h (SYNCDRV register = 0h) (when using XHS and XVS output)



Power-on/off Sequence when using SLVS-EC

1. Power-on Sequence (SLVS-EC)

Make sure that both XVS and XHS must be set to LOW while XCLR is LOW.

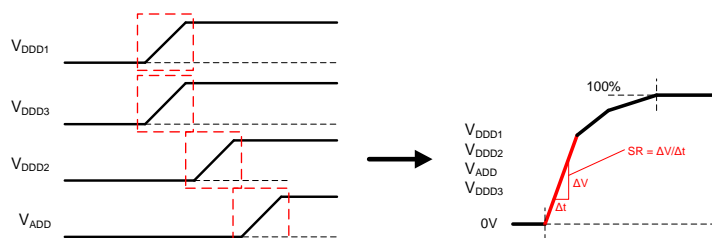


Power-on Sequence (SLVS-EC)

Period name	Remarks
(1) Power stabilization time	All input signals are Low level. There are no constraints of the power-on sequence with V_{ADD} , V_{DD1} , V_{DD2} and V_{DD3} .
(2) Standby cancel register communication	Wait 500 ns after the last power supply in V_{ADD} , V_{DD1} , V_{DD2} and V_{DD3} . Then set XCLR to "High" level and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence (SLVS-EC)

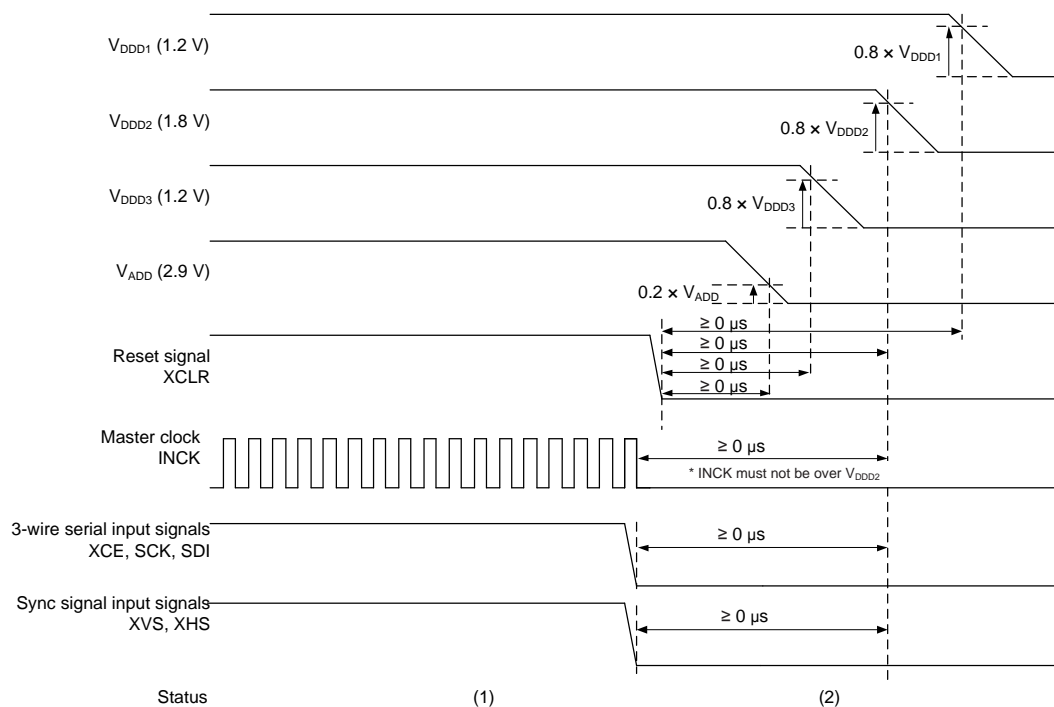
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DD1} (1.2 V)	—	25	mV/μs	
		V_{DD2} (1.8 V)	—	25	mV/μs	
		V_{DD3} (1.2 V)	—	25	mV/μs	
		V_{ADD} (2.9 V)	—	25	mV/μs	

3. Power-off Sequence (SLVS-EC)

Make sure that all input signals for the 3-wire serial interface and other signals are LOW in the period of (2) and both XVS and XHS must be set to LOW while setting XCLR to LOW.



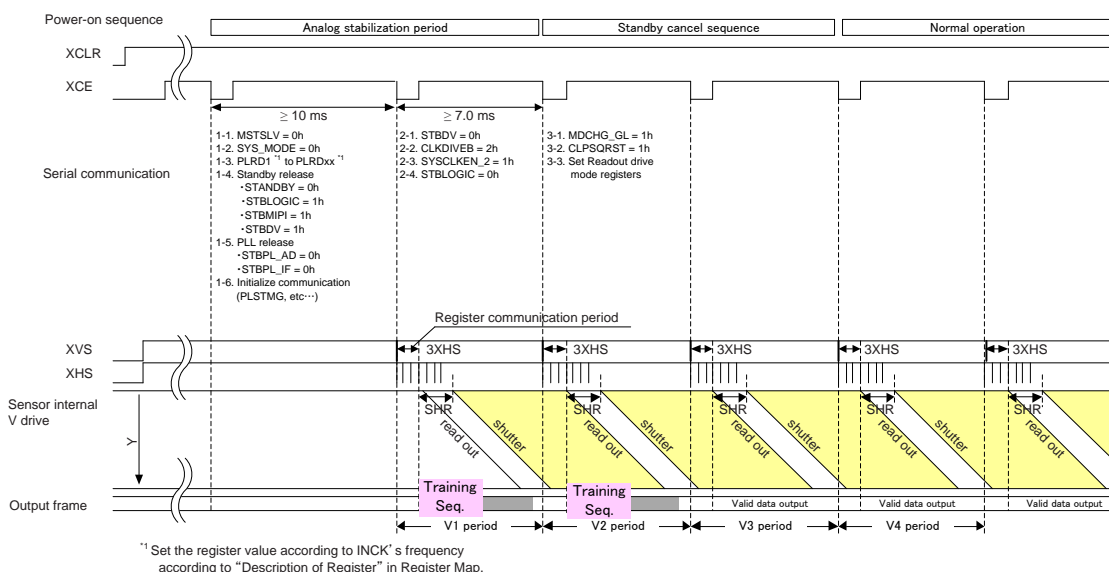
Power-off Sequence (SLVS-EC)

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off time	Turn the power supplies off after Low level is set to all input signals. There are no constraints of the power-off sequence with V_{ADD} , V_{DD1} , V_{DD2} and V_{DD3} .

Standby Cancel Sequence (SLVS-EC)

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancel sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, make the following register setting.
 - 1-1. Set address 0033h to 10h (XMSTA register = 1h, MSTSLV register = 0h)
 - 1-2. Set address 003Ch to 00h (SYS_MODE register = 0h)
 - 1-3. PLL setting
 - Set the following registers to the appropriate value according to INCK's frequency.
 - Refer to "Description of Register" of "Register Map" on page 50.
 - Address 01E8h, bit[7:0] and Address 01E9h, [7:0] (PLRD1 register)
 - Address 0122h, bit[7:0] (PLRD2 register), Address 0129h, bit[7:0] (PLRD3 register)
 - Address 012Ah, bit[7:0] (PLRD4 register), Address 011Fh, bit[7:0] (PLRD10 register)
 - Address 0123h, bit[7:0] (PLRD11 register), Address 0124h, bit[7:0] (PLRD12 register)
 - Address 0125h, bit[7:0] (PLRD13 register), Address 0127h, bit[7:0] (PLRD14 register)
 - Address 012Dh, bit[7:0] (PLRD15 register)
 - 1-4. Standby cancel
 - Set address 0000h to 1Ah (STANDBY register = 0h, STBLOGIC register = 1h, STBMDPI register = 1h, STBDV register = 1h).
 - 1-5. PLL release
 - Set address 010Bh to 00h (STBPL_IF register = 0h, STBPL_AD register = 0h).
 - 1-6. Initialize communication
 - Set all registers of PLSTMG settings.
 - See "Readout Drive Pulse Timing" on page 55. Register communication can be performed even when STANDBY is 1h and there is no restriction on the communication order.
 2. After the 1st stabilization period of 10.0 ms or more, make the following register setting.
 - 2-1. Set address 0000h to 0Ah (STANDBY register = 0h, STBLOGIC register = 1h, STBMDPI register = 1h, STBDV register = 0h).
 - 2-2. Set address 05E5h to 92h (CLKDIVEN register = 2h, SYSCLKEN register = 0h)
 - 2-3. Set address 05E5h to 9Ah (CLKDIVEN register = 2h, SYSCLKEN register = 1h)
 - 2-4. Set address 0000h to 08h (STANDBY register = 0h, STBLOGIC register = 0h, STBMDPI register = 1h, STBDV register = 0h).
 3. After the 2nd stabilization period of 7.0ms or more,
 - 3-1. Set address 0001h to 11h (MDCHGRST register = 1h, CLPSQRST register = 1h).
 - 3-2. Readout drive mode registers
 - Set the mode registers of the "Register Setting for Each Readout Drive Mode" on pages 64, 65 and 67.
 - Furthermore, set the required shutter and gain registers.
- In addition, when using the V3 period data after canceling standby mode, transmit the mode select register required for normal operation during the communication period of V2 period.



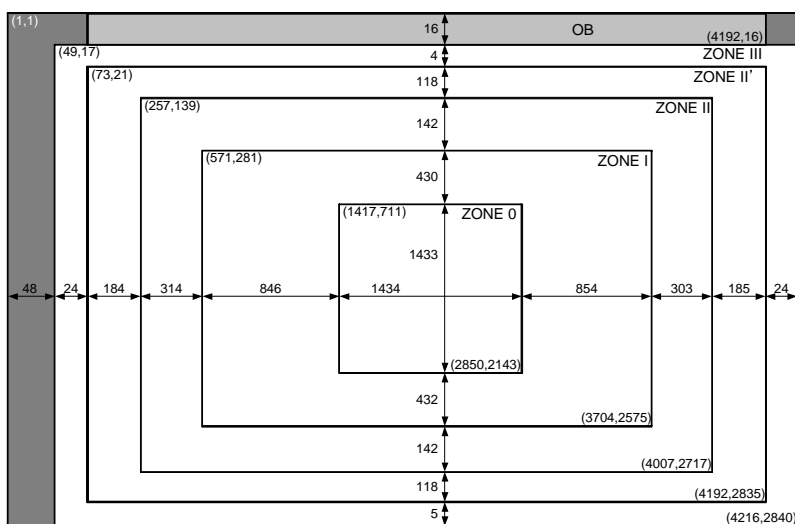
Spot Pixel Specifications

($V_{ADD} = 2.9\text{ V}$, $V_{DD1} = 1.2\text{ V}$, $V_{DD2} = 1.8\text{ V}$, $V_{DD3} = 1.2\text{ V}$, $T_j = 60\text{ }^{\circ}\text{C}$, 15 frame/s, reference gain 0 dB, MCOVGAIN = 0h (Conversion gain Low))

Type of distortion	Level	Maximum distorted pixels in each zone						Measurement method	Remarks
		0	I	II	II'	OB	III		
Black pixels at high light	$30\% \leq D$	A ^{*1}				No evaluation criteria applied		1	
White pixels at high light	$30\% \leq D$					No evaluation criteria applied		1	
White pixels in the dark	$14.1\text{ digit} \leq D \leq 27.3\text{ digit}$	B ^{*1}				No evaluation criteria applied		2	1/30 s integration
	$27.3\text{ digit} \leq D$								
Black pixels at signal saturated	$D \leq 3118\text{ digit}$	C ^{*1}				No evaluation criteria applied		3	

- Note)
- Shows digit when 12-bit output.
 - Spec of the sum of A, B and C is 2318 pixels.
 - D...Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
 - Zone definition is illustrated in the figure below.
 - 1 digit $\approx 0.237\text{ mV}$ when 12 bits output, 1 digit $\approx 0.948\text{ mV}$ when 10 bits output,

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)

Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.

Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.

Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.

The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (T _J = 60 °C)	Annual number of occurrence
5.6 mV or higher	8.9 pcs
10.0 mV or higher	5.8 pcs
24.0 mV or higher	3.0 pcs
50.0 mV or higher	1.7 pcs
72.0 mV or higher	1.3 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

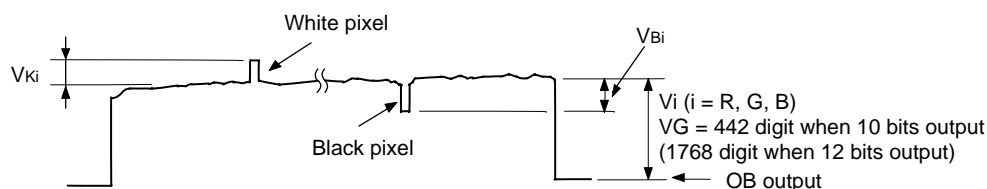
Material_No.03-0.0.10

Measurement Method for Spot Pixels

1. Black or white pixels at high light

After adjusting the luminous intensity so that the average value of the G channel signal output is 1768 digit when 12 bits output (442 digit when 10 bits output), measure the local dip point (black pixel at high light, V_{BR} , V_{BG} and V_{BB}) and peak point (white pixel at high light, V_{KR} , V_{KG} and V_{KB}) in each channel signal output. Substitute the values into the following formula.

$$\text{Spot pixel level} = (V_{Ki} \text{ (or) } V_{Bi}) / V_i \times 100 [\%] \quad (i = R, G, B)$$



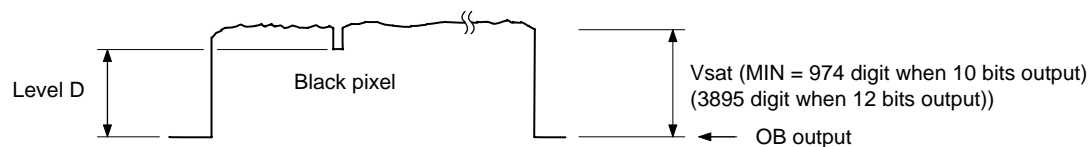
Signal output waveform of R/G/B channel (Black or White Pixels at High Light)

2. White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated

Set the device to operate in saturation and measure the local dip point in each of the R, G and B channels using the OB output with sensor as a reference.



Signal output waveform of R/G/B channel (Black Pixels at Signal Saturated)

Spot Pixel Pattern Specifications

For patterns of white pixels in the dark ($27.3 \text{ digit} \leq D$), black pixels at signal saturated ($D \leq 3118 \text{ digit}$), white pixels at high light ($30 \% \leq D$) and black pixels at high light ($30 \% \leq D$), the following table is applied.

Type of distortion	Maximum distorted pixels in each zone						Remarks
	0	I	II	II'	OB	III	
(1) Three adjacent pixels in the horizontal direction with the same color	0 spot				No evaluation criteria applied		
(2) Three adjacent pixels in the vertical direction with the same color	0 spot				No evaluation criteria applied		
(3) Two adjacent pixels in the horizontal and two adjacent pixels in the vertical with the same color	0 spot				No evaluation criteria applied		

(1) Example of three adjacent pixels in the horizontal direction with the same color


Gb	B	Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr	R	Gr

(2) Example of three adjacent pixels in the vertical direction with the same color

Gr	R	Gr	R	Gr	R	Gr	R	Gr	R
B	Gb	B	Gb	B	Gb	B	Gb	B	Gb
Gr	R	Gr	R	Gr	R	Gr	R	Gr	R
B	Gb	B	Gb	B	Gb	B	Gb	B	Gb
Gr	R	Gr	R	Gr	R	Gr	R	Gr	R
B	Gb	B	Gb	B	Gb	B	Gb	B	Gb

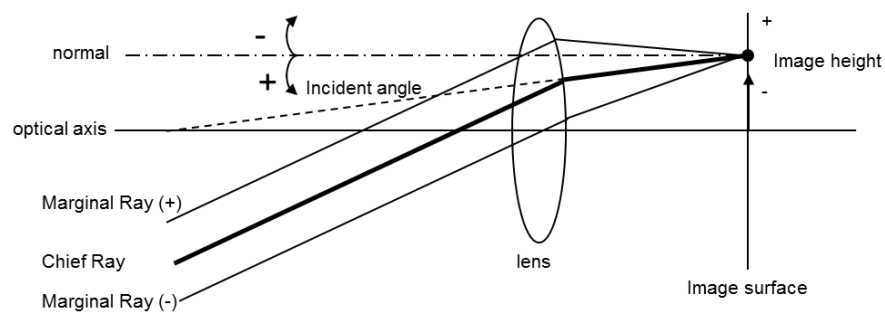
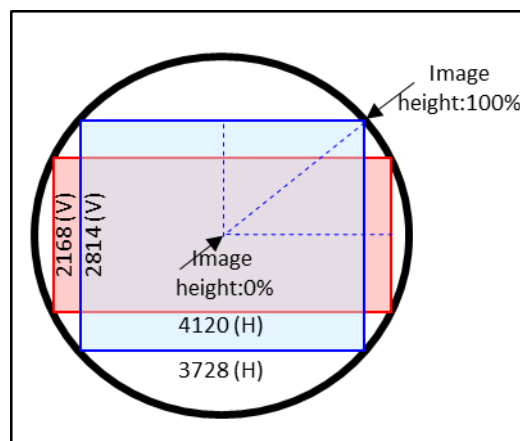
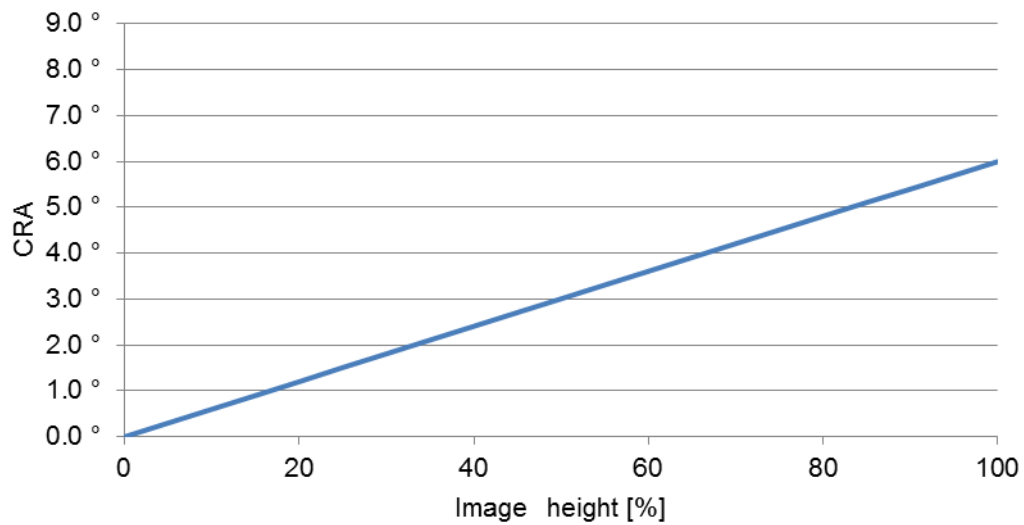
(3) Example of two adjacent pixels in the horizontal and two adjacent pixels in the vertical with the same color

R	Gr	R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B	Gb	B

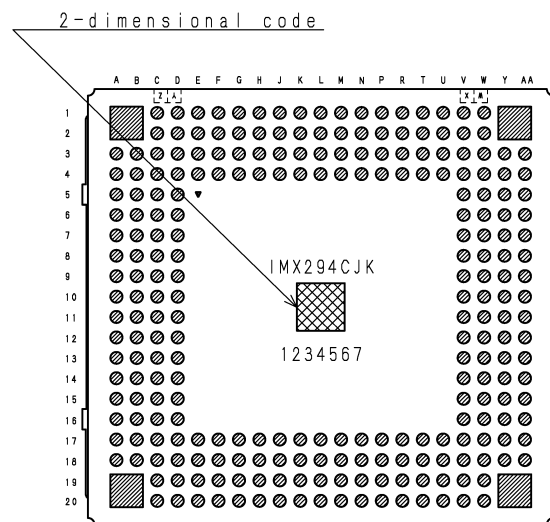
 indicates spot pixels

Relation between Image Height and target CRA

IMX294CJK CRA.VS. Image height



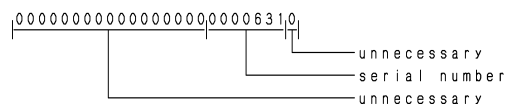
Marking



The 2-dimensional code format for serial number

1. Code Format: Data Matrix (ECC200)
2. Matrix size (2-dimensional code): 18x18
3. The details of serial number for the 2-dimensional code
The serial number for the 2-dimensional code uses the 7 digits between 18 digits and 24 digits.
(the full digits of serial number is 25 digits.)
4. Serial number consists of numbers only.

(EX.) In the case of No. 631 (serial number), describe '0000631'.



5. Alphanumeric one character is put to the W-Z part. (no plating)

DRAWING No. AM-Z294CJK (2D)

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
- (2) Use a wrist strap when handling directly.
- (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
- (4) Ionized air is recommended for discharge when handling image sensors.
- (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

- (1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
- (2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
- (3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
- (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

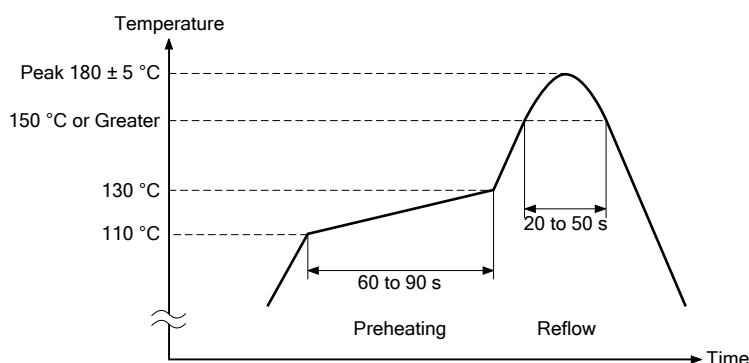
- (1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
- (2) The adhesive may cause the marking on the rear surface to disappear.
- (3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
- (4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
- (5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	110 to 130 °C 60 to 90 s
2. Temperature up (down)	±4 °C/s or less
3. Reflow temperature	150 °C or Greater 20 to 50 s Max. 5 °C/s
4. Peak temperature	Max. 180 ± 5 °C



(2) Reflow conditions

- Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 185 °C.
- Perform the reflow soldering only one time.
- Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
- Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

- Carry out evaluation for the solder joint reliability in your company.
- The paste residue of protective tape should be ignored except remarkable one.
- Note that X-ray inspection may damage characteristics of the sensor.

5. Others

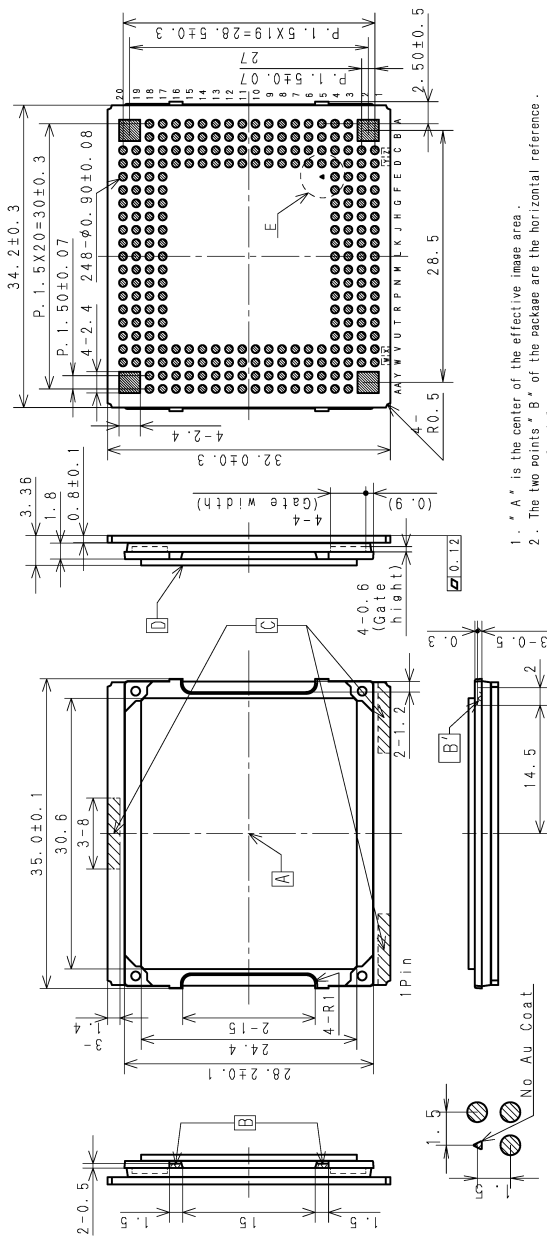
- Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
- Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
- This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
- Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
- Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.13-0.0.6

Package Outline

(Unit: mm)

248Pin LGA



1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference.
3. "C" is the height reference.
4. The center of the effective image area relative to "B" and "B'" is (H, V) = (17.50, 14.10) ± 0.30 mm
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from "C" to the effective image area is 0.6 ± 0.15 mm.
7. The height from "C" to the top of the cover glass "D" is 2.56 ± 0.15 mm.
8. The tilt of the effective image area relative to "C" is less than 150 μm.
9. The thickness of the cover glass is 0.7mm, refractive index is 1.5.
10. Glass: Both sides AR coat.
11. A resin molding course must not overflow the PKG outline.
12. One character of alphabet or number shall be placed from W to Z part. (Plating premission)

E: Detailed

PACKAGE STRUCTURE	
PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	6.8μ
PACKAGE WEIGHT	AS-275-01(E)
DRAWING NUMBER	

List of Trademark Logos and Definition Statements

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per $1 \mu\text{m}^2$ (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Data of change	Revision	Page	Contain of change
2016/04/20	0.1		First edition
2016/12/07	0.2	All	Updated references of page number Change: Quad Bayer structure name
		2	Correction: Chip Size 24.553mm(H)×20.013mm(V)
		10	Change: D6, D15 V _{DD} MPX Remark → Leave open. (No connection)
		12	Correction: Pin Description, column "A/D", W16 V _{SS} HDA, W17 V _{SS} HPX D → A
		20	Change: VDDMPX connecting to VDDD2→No connection Addition: Note, *1 V _{DD} MPX can be tied to VDDD2
		21	Correction: System Outline When Using SLVS-EC, *INCK and XHS should be synchronized → (deleted)
		31	Addition: Image Sensor Characteristics, measurement condition TBD frame/s→ 30 frame/s Addition: Item Value of G sensitivity, Sensitivity ratio, Saturation signal, Video signal shading, Dark signal, Dark signal shading, Dark signal difference, Line crawl R, Line crawl B Addition: Item Conversion Gain high/low ratio
		32-33	Addition: Image Sensor Characteristics Measurement Method, exit pupil distance, shutter speed, luminous intensity.
		35	Addition: recommended serial communication period, TBD [HMAX] → 24 [HMAX]
		43-48	Addition: Register Map, registers PLSTMG10 to 85, 101 to 104 Correction: 3017h SYNC DRV 2h: XHS/XVS is output → 0h: XHS/XVS is output Correction: 3017h[7:2] Default value 28h → 2Ah Addition: 3034h HOPBOUT_EN Addition: 3068h MDSEL15 Delete: 00DBh, 00DCh WAKEUPIF, SLEEP (Low power drive is performed automatically) Delete: 3111h SLEEP (Low power drive is performed automatically) Correction: 0114h Register Name INTI_LENGTH → INIT_LENGTH Change 3134h to 3143h Register Name PLSTMG01 to 08 → tclkpost, thszero, thsprepare, tclktrail, thstrail, tclzero, tclkprepare, tlp - Function Drive pulse timing setting 01 to 08 →Global timing register Correction: 332Ch PSSLV1, 334Ah PSSLV2 "(SLVS-EC only) Timing Setting for SLVS-EC" → Low Power Consumption Period Length (not SLVS-EC only) Addition: 357Fh to 3583h MDSEL11,12,13,14 Correction: 35B6h PSSLV3, 35B8h PSSLV4 "(SLVS-EC only) Timing Setting for SLVS-EC" → Low Power Consumption Period Length (not SLVS-EC only) Correction: 35E5h/05E5h CLKDIVEN/SYSCLEN, Address, 355Eh/055Eh → 35E5h/05E5h Addition: 36BCh PSSLV0 Delete: 3F00h to 3FFAh

Data of change	Revision	Page	Contain of change
2016/12/07	0.2	52	Addition: Description of Register, Conversion Gain, notes on setting range of analog gain and others.
		54	Addition: Description of Register, Low Power Consumption Period Length Correction: Readout Drive Mode, MDSEL1 to 10 → MDSEL1 to 15 PSSLVS1 to 4 → PSSLVS0 to 4
		55	Delete: Readout Drive Pulse Timing PLSTMG01 to 08 (Their function(global timing) is opened, their names are changed and moved to page 56) Addition: PLSTMG10 to 85, 101 to 104
		56	Addition: Global Timing Registers
		59	Delete: Description of Register, SLVS-EC I/F Standby Control
		62 to 67	Addition: Description of Register Setting for Each Readout Drive Modes, 3034h to 3039h HOPBOUT_EN, HTRIMMING_EN, HTRIMMING_START, HTRIMMING_END Addition: 3068h MDSEL15 Addition: 357Fh to 3583h MDSEL11,12,13,14 Addition: 36BCh PSSLVS0
		62	Correction: Description of Register Setting for Each Readout Drive Modes(CSI-2), SHR, address, 302Ch, 303Ch → 302Ch, 302Dh Addition: 332Ch PSSLVS1, 334Ah PSSLVS2, 35B6h PSSLVS3, 35B8h PSSLVS4
		63	Correction: Description of Register Setting for Each Readout Drive Modes(CSI-2), SHR, address 302Ch, 303Ch → 302Ch, 302Dh Addition: 332Ch PSSLVS1, 334Ah PSSLVS2, 35B6h PSSLVS3, 35B8h PSSLVS4 Correction: 3846h Register name MDSEL8 → MDSEL9 Correction: 384Ah Register name MDSEL9 → MDSEL10
		64	Correction: Description of Register Setting for Readout Drive Modes (SLVS-EC) SHRaddress 002Ch, 003Ch → 002Ch, 002Dh Correction: MDSEL8, address, 008Ah → 00A8h
		65	Correction: Description of Register Setting for Readout Drive Modes (SLVS-EC) SHRaddress 002Ch, 003Ch → 002Ch, 002Dh Correction: MDSEL8, address, 008Ah → 00A8h
		66	Correction: Description of Register Setting for Readout Drive Modes (CSI-2) SHRaddress 302Ch, 303Ch → 302Ch, 302Dh Addition: 332Ch PSSLVS1, 334Ah PSSLVS2, 35B6h PSSLVS3, 35B8h PSSLVS4
		67	Correction: Description of Register Setting for Readout Drive Modes (SLVS-EC) SHRaddress 002Ch, 003Ch → 002Ch, 002Dh Correction: MDSEL8, address, 008Ah → 00A8h Correction: 0846h, Register name, MDSEL8 → MDSEL9 Correction: 084Ah, Register name, MDSEL9 → MDSEL10
		79	Correction: Horizontal Operation Period in Each Readout Drive Mode, Front ignored area → 0 HMAX register minimum value, updated in all modes Addition: column "HMAX number per H period"

Data of change	Revision	Page	Contain of change
2016/12/07	0.2	80	Correction: Examples of HMAX, VMAX and Frame Rate HMAX register minimum value, Max frame frequency → updated in all modes Correction: NTSC compatible drive, mode1B, note *3 → (delete)
		82 to 85	Change Readout Pixel Image Diagram of all modes, Front ignored area → (delete)
		86	Correction: Horizontal Operation Period in Each Readout Drive Mode, Front ignored area → 0 HMAX register minimum value updated in all modes Addition: column "HMAX number per H period"
		87	Correction: Examples of HMAX, VMAX and Frame Rate HMAX register minimum value, Max frame frequency updated in all modes Change: NTSC compatible drive, mode0, 29.97 frame/s → 24.00 frame/s *3 Addition: note *3 The frame rate is not compatible for NTSC
		88 to 89	Change: Readout Pixel Image Diagram of all modes, Front ignored area → (delete)
		92	Addition: Vertical Minimum Period When Using Vertical Arbitrary Cropping Function, formula and example of calculation (table was deleted)
		93	Correction: Table HNUM value, mode No. 0,1,2A,7,10 → 0,1,1A,7,10
		94	Addition: Table HMAX Minimum Value When Using Horizontal Arbitrary Cropping Function, all modes are updated from TBD
		95	Correction: Shutter Control Register Setting Range (CSI-2), Readout mode No.11 5 to {(SVR value + 1) × Number of XHS pulses per frame - 1} → 5 to {(SVR value + 1) × Number of XHS pulses per frame / 4 - 1}
		97	Addition: Table Number of clocks per internal offset period, all modes are updated from TBD
		(100)	Delete: Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation (Low power drive is performed automatically)
		105	Correction: Horizontal Operation Period in Each Readout Drive Mode, Front ignored area → 0 XHS minimum period updated in all modes Addition: column "XHS number per H period" Correction: Vertical Operation Period in Each Readout Drive Mode - Vertical front blanking: updated in all modes, and both H number and XHS number are noted. - XVS minimum period: mode4 1108→1109 / mode6 1108→1109 / mode8 1126→1131 / mode10 265→267 / mode11 258→255
		106	Delete: Table "H Period and Number of XHS Pulses, V Period and XVS Pulses" - XHS number in H period is added to the table "Horizontal Operation Period in Each Readout Drive Mode" on page105. Correction: Examples of XHS Period, XVS period and Frame Rate - XHS minimum period and max frame frequency: updated in all modes Addition: mode11, note *2 Low power consumption drive (SVR = 7h).

Data of change	Revision	Page	Contain of change
2016/12/07	0.2	108 to 120	Change: Readout Pixel Image Diagram of all modes, Front ignored area → (delete) Vertical front blankings are updated in all modes Addition: Readout Drive Timing to all modes
		121	Correction: Horizontal Operation Period in Each Readout Drive Mode, Front ignored area → 0 XHS minimum period updated in all modes Addition: column "XHS number per H period" Correction: Vertical Operation Period in Each Readout Drive Mode - Vertical front blanking: updated in all modes, and both H number and XHS number are noted. - XVS minimum period, mode10, 331→335
		122	Delete: Table "H Period and Number of XHS Pulses, V Period and XVS Pulses" - XHS number in H period is added to the table "Horizontal Operation Period in Each Readout Drive Mode" on page121. Correction: Examples of XHS Period, XVS period and Frame Rate - XHS minimum period and max frame frequency: updated in all modes Correction: frame frequency, mode0, 29.97 → 24.00 *2 Addition: note *2 The frame rate is not compatible for NTSC.
		123 to 127	Change: Readout Pixel Image Diagram of all modes, Front ignored area → (delete) Vertical front blankings are updated in all modes Addition: Readout Drive Timing to all modes
		130	Addition: Vertical Minimum Period When Using Vertical Arbitrary Cropping Function, formula and example of calculation (table was deleted)
		131	Correction: Table HNUM value, mode No. 0,1,2A,7,10 → 0,1,1A,7,10
		132	Addition: Table HMAX Minimum Value When Using Horizontal Arbitrary Cropping Function, all modes are updated from TBD
		133	Correction: Shutter Control Register Setting Range (SLVS-EC), Readout mode No.11 5 to {(SVR value + 1) × Number of XHS pulses per frame - 1} → 5 to {(SVR value + 1) × Number of XHS pulses per frame / 4 - 1}
		135	Addition: Table Number of clocks per internal offset period, all modes are updated from TBD
		138	Addition: Table "Integration Start Time of the Exposure Start Period" TBDs are updated
		139	Delete: Low Power Consumption Drive in Exposure of Global Reset Shutter Operation Sequence (Low power drive is performed automatically)
		140	Correction: Figure Frame Format of Interruptive Mode Change - HiZ period is added before Low period
		(141)	Delete: Polygon 1st Curtain Electronic Shutter Mode
		141	Addition: Figure Power-on Sequence(CSI-2), restrictions when SLASEL is to be driven to H.
		142	Addition: Figure Power-off Sequence(CSI-2), restrictions when SLASEL is driven to H.

Data of change	Revision	Page	Contain of change
2016/12/07	0.2	143	Change: Standby Cancel Sequence when using CSI-2 (whole), replaced partial bit notation to whole byte notation. Correction: 1-1, Register name XMASTA → XMSTA Correction: 2-2, address 355Eh → 35E5h Correction: step 2-2, 2-3 - explicitly write the order of CLKDIVEN=0→2 and SYSCLKEN=0→1. (These 2 settings must be done separately) Correction: note within figure, *1 Register Map → datasheet
		146	Change: Standby Cancel Sequence when using SLVS-EC (whole), replaced partial bit notation to whole byte notation. Correction: 1-1 Register name XMASTA → XMSTA Correction: step 2-2, 2-3 - explicitly write the order of CLKDIVEN=0→2 and SYSCLKEN=0→1. (These 2 settings must be done separately) Correction: 3-1,3-2 combined 2 writing to the same address 0001h. Correction: Within figure, Register name CLKDIVEB → CLKDIVEN Correction: Within figure, note *1 Register Map → datasheet
2017/04/24	E17405	22	Added: Current Consumption and Gain Variable Range (CSI-2) Max Current consumption and Max Standby current are added.
		25	Added: Current Consumption and Gain Variable Range (SLVS-EC) Max Current consumption and Max Standby current are added.
		30	Addition: Spectral Sensitivity Characteristics
		48	Addition: Address 3600h / 0600h, register MDSEL16 Address 36C4h / 06C4h to 36C6h / 06C6h, register PLSTMG105 to PLSTMG107
		54	Addition: Low Power Consumption Period Length Add a note "or V _{BLK} is too small and some of setting value cannot be calculated"
		55	Addition: Address 36C4h / 06C4h to 36C6h / 06C6h register PLSTMG105 to PLSTMG107
		62 to 67	Correction: Description of Register Setting for Readout Drive Modes 1 to 4 non-used bit of address 3039h / 0039h: [6:5] → [7:6] Addition: register MDSEL16 (address 3600h / 0600h)
		66	Correction: Description of Register Setting for Each Readout Drive Modes (CSI-2) mode1, MDSEL16(3600h) 007Dh → 0090h mode1A, MDSEL16(3600h) 0090h → 007Dh
		67	Correction: Description of Register Setting for Each Readout Drive Modes (SLVS-EC) mode1, MDSEL16(0600h) 007Dh → 0090h mode1A, MDSEL16(0600h) 0090h → 007Dh
		68	Correction: Description of Readout Drive Modes mode No. 1A, 2A: Low power consumption → low noise
		69	Correction: Description of Readout Drive Modes mode No. 1A: Low power consumption → low noise

Data of change	Revision	Page	Contain of change
2017/04/24	E17405	73	Changed: Table "DATA Type" Node *1, changed document's name: IMX294 Application Note Digital Overlap HDR → IMX294 Application Note Quad Bayer Coding HDR
		79	Correction: Horizontal Operation Period in Each Readout Drive Mode Rear ignored area of effective pixel mode No. 1A, 2A: 24 → 32 / mode No. 3 to 7: 12 → 16 / mode No. 8 to 11: 8 → 12 XHS minimum period updated in all modes HMAX number per H period, mode No. 11: 1 → 4 Vertical Operation Period in Each Readout Drive Mode, XVS minimum period mode No.11: 255 → 257
		80	Correction: Examples of XHS Period, XVS period and Frame Rate, XHS minimum period mode No. 1: 1098 → 1122 / mode No. 1B: 1030 → 1055 / mode No. 2: 925 → 947 / mode No. 2A: 930 → 954 / mode No. 5: 583 → 607 Max frame frequency, mode No. 1: 58.97 → 57.76 / mode No. 1B: 62.86 → 61.43 / mode No. 2: 69.67 → 68.13 / mode No. 2A: 69.30 → 67.63 / mode No. 5: 107.39 → 103.32 NTSC compatible drive, HMAX, mode 5: 600 → 616 NTSC compatible drive, VMAX, mode 5: 2002 → 1950
		82	Correction: Readout Image Diagram, mode No.1A, 2A, low power consumption → low noise Horizontal total output pixels: 4168 → 4176 Horizontal rear ignored area of effective pixels: 24 → 32
		83	Correction: Readout Image Diagram, mode No.3, 4, 5, Horizontal total output pixels: 2084 → 2088 Horizontal rear ignored area of effective pixels: 12 → 16
		84	Correction: Readout Image Diagram, mode No.6, 7, Horizontal total output pixels: 2084 → 2088 Horizontal rear ignored area of effective pixels: 12 → 16 Correction: Readout Image Diagram, mode No.8, 9, Horizontal total output pixels: 1388 → 1392 Horizontal rear ignored area of effective pixels: 8 → 12
		85	Correction: Readout Image Diagram, mode No.10, 11, Horizontal total output pixels: 1388 → 1392 Horizontal rear ignored area of effective pixels: 8 → 12
		86	Correction: Horizontal Operation Period in Each Readout Drive Mode, HMAX register minimum value, mode No. 1: 1010 → 1034
		87	Correction: Examples of XHS Period, XVS period and Frame Rate, HMAX register minimum value, mode No. 1: 1010 → 1034 Max frame frequency, mode No. 1: 49.32 → 48.22 PAL compatible drive, mode0: XHS period = 1600, XVS period = 1800 → XHS period = 1800, XVS period = 1600
		88	Correction: mode1A, low power consumption → low noise

Data of change	Revision	Page	Contain of change
2017/04/24	E17405	95	Correction: Shutter Control Register Setting Range (CSI-2), Register Value Readout mode no.1A, 2A: low power consumption → low noise
		101	Changed: Table "Contents of Header", Data ID changed document's name IMX294 Application Note Digital Overlap HDR → IMX294 Application Note Quad Bayer Coding HDR
		102	Correction: Frame Format (Invalid frame with training sequence) After Standby Sequence HiZ period is added.
		105	Correction: Horizontal Operation Period in Each Readout Drive Mode, Rear ignored area of effective pixel mode No. 1A, 2A: 24 → 32 / mode No. 3 to 7: 12 → 16 / mode No. 8 to 11: 8 → 12 XHS minimum period updated in mode No. 1A to 11 Vertical Operation Period in Each Readout Drive Mode, XVS minimum period mode No.11: 255 → 257
		106	Correction: Examples of XHS Period, XVS period and Frame Rate, XHS minimum period, Max frame frequency mode No. 1: 706 → 725 / mode No. 10: 709 → 743 / mode No. 11: 590 → 520 XVS minimum period, mode No. 4, 6: 1108 → 1109 / mode No. 8: 1126 → 1131 mode No. 10: 265 → 267 / mode No. 11: 258 → 257 NTSC compatible drive, XHS period, mode No. 1: 715 → 728 mode No. 10: 715 → 770 XVS period, mode No. 1: 1680 → 1650 mode No. 10: 336 → 312 PAL compatible drive, XHS period, mode No. 10: 720 → 800 XVS period, mode No. 10: 400 → 360 mode1 92.13 → 89.71 / mode4 92.04 → 91.96 / mode6 124.97 → 124.85 mode8 122.97 → 122.42 / mode10 383.21 → 362.94 / mode11 59.12 → 67.35
		107	Correction: Imaging Conditions in Each Readout Drive Mode Number of horizontal recording pixels, mode No.8 and 9: 1376 → 1364
		108	Correction: Readout Drive Timing, XVS Period 1680 → 1650 XHS Period 715 → 728
		109, 111	Correction: mode description: low power consumption → low noise Correction: Readout Image Diagram, Horizontal total output pixels: 4168 → 4176 Horizontal rear ignored area of effective pixels: 24 → 32 Correction: Readout Drive Timing Horizontal output part (lower half) is revised
		112 to 116	Correction: Readout Image Diagram, Horizontal total output pixels: 2184 → 2188 Horizontal rear ignored area of effective pixels: 12 → 16 Correction: Readout Drive Timing Horizontal output part (lower half) is revised
		117 to 120	Correction: Readout Image Diagram, Horizontal total output pixels: 1388 → 1392 Horizontal rear ignored area of effective pixels: 8 → 12 Correction: Readout Drive Timing Horizontal output part (lower half) is revised

Data of change	Revision	Page	Contain of change
2017/04/24	E17405	122	Correction: Examples of XHS Period, XVS period and Frame Rate, XHS minimum period mode10: 331 → 335 PAL compatible drive, mode0: XHS period = 1600, XVS period = 1800 → XHS period = 1800, XVS period = 1600 Correction: Examples of XHS Period, XVS period and Frame Rate (SLVS-EC), Max frame frequency mode10 418.31 → 413.32
		125	Correction: mode description: low power consumption → low noise
		132	Correction: XHS Minimum Period When Using Horizontal Arbitrary Cropping Function mode No. 0: 706 → 1730 mode No. 1: 1192 → max(706, [HTRIMMING_END – HTRIMMING_START] × 1/6 + 34.0) mode No. 1A: 520 → 1192 / mode No. 2: 827 → 520 / mode No. 2A: 706 → 827 / mode No. 4: 520 → 706 / mode No. 10: ...+14.0 → ...+46.0 mode No. 11: max(520, [HTRIMMING_END – HTRIMMING_START] × 5/36 + 11.0) → 520
		133	Correction: Shutter Control Register Setting Range (SLVS-EC), Register Value Readout mode no.1A, 2A: low power consumption → low noise Changed: Shutter Control Register Setting Range Global reset shutter mode (SMD=1): TBD → 43
		138	Changed: the minimum XVS period is TBD XHS → 15 XHS Changed: Possible Integration Time Range of Global Reset Shutter → Possible Length of XVS period in Integration Frame of Global Reset Shutter and values are updated.
		140	Changed: “after TBD XHS or more” → 15 XHS Note *1 (mode No. 11), “wait TBD XHS periods or more” → 51 XHS
		143	Added: setting step 1-6. Set all registers of PLSTMG → 1) Set all registers of PLSTMG and 2) Set all of Global Timing Registers
		146	Correction: setting step 2 period of 7.0 ms or more → period of 10.0 ms or more Correction: In the timing chart below Training Sequence are added at V1 period and V2 period.
		147	Correction: Level, Black pixels at signal saturated, 3277 digit → 3118 digit
		149	Correction: Black pixels at signal saturated, in the figure, MIN=1023 digit → 974 digit (10 bits output), 4097 digit → 3898 digit (12 bits output)
		147 to 150	Added: Spot pixel specifications are updated

Data of change	Revision	Page	Contain of change
2017/04/24	E17405	150	Correction: level of black pixels at signal saturated, 3277 digit → 3118 digit level of while pixels at high light, 13 % → 30 %, level of black pixels at high light, 13 % → 30 %
		152	Added: Marking
2017/09/07	E17405A79	20	Correction: peripheral circuit
		31	Correction: frame rate 30 frame/s → 15 frame/s Saturation signal 4097 → 4095
		62	Correction : Description of Register Setting for Each Readout Drive Modes (CSI-2) Mode2, MDSEL16(3600h) 007Dh → 0090h Mode2A, MDSEL16(3600h) 0090h → 007Dh
		74,75	Correction : Embedded data line format Data format code 0Ah deleted
		80	Correction :Mode1B NTSC setting HMAX 1040 →1200 VMAX 1155 →1250 Frame frequency 59.94 →48.00
		90 to 92	Correction: Vertical arbitrary cropping function (CSI-2) VWIDCUT: Veff – VWIDCUT x 2 → Veff – VWIDCUT x step VWIDPOS: VWINPOS x 2 → VWINPOS x step
		128 to 130	Correction: Vertical arbitrary cropping function (SLVS-EC) VWIDCUT: Veff – VWIDCUT x 2 → Veff – VWIDCUT x step VWIDPOS: VWINPOS x 2 → VWINPOS x step
		141	Correction: Power-on sequence (CSI-2) INCK input timing INCK can be input earlier than XCLR = H
		144	Correction: Power-on sequence (SLVS-EC) INCK input timing INCK can be input earlier than XCLR = H
		147	Correction: frame rate 30 frame/s → 15 frame/s
		149	Correction : Signal output waveform of R/G/B channel figure 3898 → 3118
2017/12/25	E17405B7Z	18	Correction: DMOxP, DMOxM, DCKP, DCKM Circuit diagram is corrected to the one with protection diode Correction: DOPx, DOMx Circuit diagram is corrected to the one with protection diode
		23	Changed: AC Characteristics(CSI-2), INCK Low level pulse width (twl) Criteria 10% → 0.3×V _{DD2} Changed: AC Characteristics(CSI-2), INCK High level pulse width (twh) Criteria 90% → 0.7×V _{DD2} Addition: AC Characteristics, Clock duty, Remark, Criteria is 0.5×V _{DD2}
		25	Changed: Supply Voltage and I/O Voltage(SLVS-EC), Digital input voltage V _{IH} Min.: 0.8×V _{DD2} → 0.7×V _{DD2} V _{IL} Max.: 0.2×V _{DD2} → 0.3×V _{DD2}

Data of change	Revision	Page	Contain of change
2017/12/25	E17405B7Z	27	<p>Changed: AC Characteristics(SLVS-EC), INCK Low level pulse width (twl) Criteria is changed from 10% to $0.3 \times V_{DD2}$</p> <p>Changed: AC Characteristics(SLVS-EC), INCK High level pulse width (twh) Criteria is changed from 90% to $0.7 \times V_{DD2}$</p> <p>Addition: AC Characteristics, Clock duty, Remark, Criteria is $0.5 \times V_{DD2}$</p>
		144	<p>Correction: Power-on sequence (SLVS-EC) XVS, XHS timing XVS, XHS can be set to H earlier than XCLR = H</p>
		145	<p>Correction: Power-off sequence (SLVS-EC) XVS, XHS timing XVS, XHS can keep H after XCLR=L</p>
		148	<p>Changed: Notice on White Pixels Specifications cosmic radiation → particle radiation such as cosmic rays etc. Sony Corporation → Sony Semiconductor Solutions Corporation “The annual number of White Pixels occurrence at an altitude...” → (removed)</p>
		155	<p>Correction: Package Outline note 4 (17.05, 14.10) → (17.50, 14.10) (The value 17.05 is unintentional error only in ver. E17405 and . Ver. E17405A79 and previous versions have correct value. (=17.50))</p>